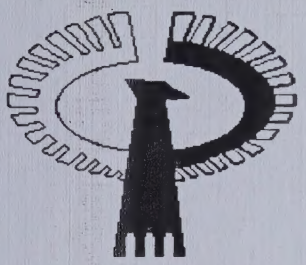


Phoenix

Phoenix Instruction Book

5500
Data Communications Analyzer

Engineering New Standards in Technology

Phoenix

Phoenix microsystems, inc.
991 DISCOVERY DRIVE
HUNTSVILLE, ALABAMA 35806
TEL: (205) 721-1200 FAX: (205) 837-1256 TELEX: 752592

November 11, 1988

To: Our Valued Customer

Subj: Instruction Manual for Your 5500

Due to a problem at our printer, the 5500 Instruction Manuals are temporarily out of stock. The manuals should arrive at Phoenix within the next ten days.

It is normal Phoenix policy to hold delivery of equipment until the order includes an instruction manual. However, in this case we are sending you the equipment along with a temporary copy of the instruction manual. We hope that this will enable you to begin familiarization with your 5500. We will ship your instruction manual to you via Federal Express the day we receive them from our printer.

If you have any problems or questions about your 5500 before you receive your instruction manual, please call me, Russ Bryant, at 1-800 826-6798 Ext 201. I will do my best to assist you with your questions.

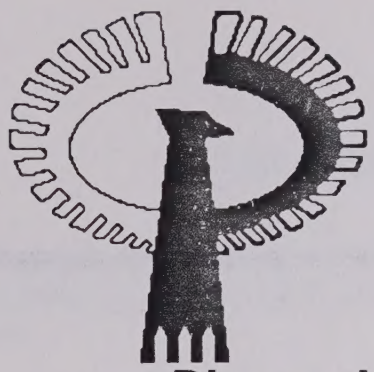
Again, please accept my apologies for this inconvenience Your patience and understanding in this matter are appreciated.

Sincerely,

Russ Bryant
Director of Sales

Front Foot #

(H) 9-5500A-5000-1



Phoenix

microsystems, inc.

Phoenix Instruction Book

October 1, 1987

5500

Data Communications Analyzer

This instruction book includes:

Introduction

Description

Installation

Operation

Application

Application Notes

Maintenance

Options

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Phoenix microsystems, inc.
991 Discovery Drive
Huntsville, Alabama 35806

WARRANTY

Phoenix Microsystems warrants each Model 5500 and options against defects in material and workmanship for a period of one year from the date the Model 5500 was shipped to the customer. If at any time during the warranty period, the Model 5500 should malfunction, Phoenix will repair, or at Phoenix's option, replace the unit free of charge. The remedies listed herein are the users sole and exclusive remedies. Phoenix microsystems, inc. shall not be liable for any indirect, direct, incidental, or consequential damages. Owner must return the unit to the factory, shipping prepaid and packaged to best commerical standard for electronic equipment. Phoenix will pay shipping charges for delivery on return. Customer is responsible for mode and cost of shipment to Phoenix.

Warraanty does not apply if the unit has beeen damaged by accident, misuse or as a arresult of service or modification by other than Phoenix personnel.

The warranty registration card, shipped with the equipment, must be completed and returned to Phoenix microsystems, inc. to validate the warranty.

DESIGN FEATURES

The Model 5500 Communications Data Analyzer is the most powerful and versatile data communications analyzer in its class. It will measure BERT error performance parameters, plus frequency, bias distortion, event time, and (optional) phase jitter simultaneously. Among the features of the 5500 are:

* Adaptable, tests framed and unframed test patterns including ESF and SLC®96.

* Versatile, software control permits variety of standard and user input patterns and programs.

* Remote programming, RS-232 and IEEE-488 control ports standard.

* Modular, plug-in interface modules have full DCE/DTE capability.

* Available version (5501) tests to CCITT G.821 Error Performance Standards for ISDN.

* Selectable bit error and bipolar violation injection capability.

* Graphic display of any one of nine error parameters verses time for up to 60 hours in one minute intervals.

Phoenix Model 5500 Data Communications Analyzer

SLC96 is a registered trademark of AT&T

INSTRUCTION BOOK

The 5500 Communications Data Analyzer instruction book includes all the instructions on the basic unit and supports operation of the basic unit. Included are any supplements necessary to define and support different configurations of the 5500. The Option section of this instruction manual includes the instructions for the various options that are available for the 5500.

Changes and revisions to the Model 5500 instruction manual are printed as required to keep the manual current with software and hardware revisions. To ensure you receive your copy of these changes/revisions, be sure to fill out and return the publication registration card inserted in this book. If the card is missing, send a letter with your name and mailing address, the date you received your 5500 and the serial number of the 5500 to:

Manager Technical Publications
Phoenix microsystems, inc.
991 Discovery Drive
Huntsville, AL 35806
1-800 826 6798 Ext 213

WARRANTY

As a registered owner, you have available the following benefits during the warranty period: software or hardware updates to correct 'bugs'; software updates that enhance operation of the equipment; updates and changes to the instruction book; technical alert bulletins; and five day repair service on any equipment failure.

For warranty work or questions about your equipment contact:

Customer Service Manager
Phoenix microsystems, inc.
991 Discovery Drive
Huntsville, Alabama 35806

Telephone: 1-800 826-6798 USA
(205) 721-1200

Telex #: 752592 (PMIHTBV)
FAX: (205) 837-1256

When returning your unit for warranty work, a Return Material Authorization (RMA) number must be obtained from customer service at the above address/phone number. When calling Phoenix microsystems to obtain a returned material authorization number, or to arrange service, it will expedite matters if you will have the following information available when you call:

a. Model number(s) and serial number(s) for the unit(s).

b. Reason for return/symptoms of problem.

c. Warranty status (if known).

d. Purchase order number to cover charges for out-of-warranty items.

e. Name and phone number of person we can contact if we have questions about the unit(s).

f. Mode of shipment required. (2nd day air is normal mode of shipment for all returned material unless otherwise specified.)

As soon as Phoenix microsystems has the above information, the RMA, that must accompany the item(s) being returned, can be issued.

5500
Data Communications Analyzer

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Phoenix Instruction Book

34-00015-121TB
2nd Edition, 15 October 1987
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1.1 SPECIFICATIONS.....1-1
1.2 EQUIPMENT SUPPLIED.....1-6
1.3 OPTIONS.....1-6

1.0 GENERAL

This section contains technical information on the Model 5500 Data Communications Analyzer. The Model 5500 is the most comprehensive and advanced error rate and phase jitter test set presently available. While the Model 5500 will perform complex testing, it is a simple, straightforward instrument to use. The software driven menus and programmability of the Model 5500 make one button testing a reality.

1.1 SPECIFICATIONS

Table 1-1 presents the specifications for the Model 5500.

Table 1-1. Model 5500 Specifications.

BIT RATES

Low Speed Modules

75,110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3200, 3600, 4800, 6400, 7200, 8000, 9600, 14.4K, 16K, 19.2K, 24K, 28.8K, 32K, 48K bps - synchronous and asynchronous

56K, 57.6K, 64K, 72K, 76.8K, 84K, 96K, 112K, 115.2K, 128K, 144K, 153.6K, 168K, 192K, 224K, 230.4K, 256K, 288K, 336K, 384K, 448K, 460.8K, 512K, 576K, 672K, 768K, 1024K, 1544K bps - synchronous

High Speed Modules

1.544Mbps, 2.048Mbps, 3.152Mbps, 6.312Mbps, 8.448Mbps

CLOCK SOURCES

Internal Clock (see bit rates above)
User Clock (User supplied TTL clock - 50 bps to 13Mbps)
External Clock (Clock supplied by interface module - TC, RC, XC, etc.)
Recovered Clock (Clock recovered from received bit stream)

Table 1-1. Model 5500 Specifications (Cont.).

PATTERNS

Mark	511
Space	SYSY 511
Alt	X25 511
TSET	2047
TRESET	REV 2047
63	2^15-1
QRW	2^20-1
FOX	

USER - 3 user programmable patterns aof 24 to 1080 bits
1 user programmable pattern of 24 to 16384 bits.

PATTERN SYNC CRITERIA

To accquire pattern synchronization:

For MARK, SPACE, ALAT, FOX, TSET, TRESET: 56 consecutive error free bits.

For 63, 511, 2047, REV 2047, 2^15-1, 2^20-1, QRW: A number or error free bits length of 24+x for a 2^x-1 pattern.

For SYSY 511 and X25 511: Entire pattern error free (over 4000 bits).

Loss of pattern synchronization

Adjustable - factory setting of 100 bit errors in a 1000 bit test block. (can be set from 1 bit error to 896 bit errors in a 1000 bit test block.

INJECTABLE ERROR RATES

Bit Errors	9E-3 to 1E-9
BPVs	9E-3 to 1E-7
CRC	9E-3 to 1E-7
F-Bit	9E-3 to 1E-7
S-Bit	9E-3 to 1E-7
Bit errors in live traffic	9E-3 to 1E-7

Single error inject available on all of the above

Table 1-1. Model 5500 Specifications (Cont.).

TEST RESULTS

Numeric Results

ABE	Adjusted Bit Errors
ABER	Adjusted Bit Error Rate
BE	Bit Errors
BER	Bit Error rate
BLE	Block Errors
BLK	Blocks
BITS	Bits Analyzed
CBE	Current Bit Errors
CBER	Current Bit Error Seconds
CRCE	CRC Errors
CRER	CRC Error Rate
CSLP	Clock Slips (measured in bit times)
EBR	Errored Block Rate
EFB	Error Free Blocks
FBE	Frame Bit Errors
FBER	Frame Bit Error Rate
FLOS	Occurences of Frame Losses
LOS	Pattern Sync Loss
PF	Power Failures
RBPV	Received Bipolar Violations
RVR	Receive BPV Rate
RSL	Receiver Sync Losses
TBPV	Transmitter Bipolar Violations
TVR	Transmitter Bipolar Violation Rate
TSL	Transmitter Sync Losses
WND+	Positive Peak Wander
WND-	Negative Peak Wander
15Z	Occurences of greater than 15 consecutive zeros
%1sD	Percent Ones Density (ones/bits)

Time Based Results

BALS	Blue Alarm Seconds
CRES	CRC Errored Seconds
CEFS	CRC Error Free Seconds
ET	Elapsed Test Time
ED	Elapsed Test Days
ETS	Elapsed Test Time in Seconds
ES	Errored Seconds
EFS	Error Free Seconds

Table 1-1. Model 5500 Specifications (Cont.).

Time Based Results (Cont.)

ESR	Errored Second Rate
EFS%	Percent of Error Free Seconds (EFS/ETS)
FBES	Frame Bit Errored Seconds
FEFS	Frame Bit Error Free Seconds
FLS	Frame Loss Seconds
MDY	Month Day Year
RSLS	Receiver Sync Loss Seconds
RVS	Receiver BPV Seconds
RVFS	Receiver BPV Free Seconds
SLS	Pattern Sync Loss Seconds
TES	Total Elapsed Seconds
TOD	Time of Day
TSLS	Transmitter Sync Loss Seconds
TSS	Transmitter Sync Seconds
TVS	Transmitter BPV Seconds
TVFS	Transmitter BPV Free Seconds
YALS	Yellow Alarm Seconds
15ZS	Seconds of >15Z

Special Results

ALRM	Alarm Status
AHST	Alarm History

FREQUENCY MEASUREMENT

Measurement Selections: TC - Transmit Clock
RC - Receive Clock
XC - External Clock
BR - Bit Rate

Measureament Range: 150 Hz to 16 MHz

Measurement Accuracy: ±.0005% ± LSD

Table 1-1. Model 5500 Specifications (Cont.).

EVENT TIMING (Low Speed Modules)

Start/Stop Sources: TD, RD, CTS, RTS, DCD, DSR, DTR, SQ
Either rising or
falling edge

Measurement Range: 1 usec to 4.67 minutes

Resolution: ± 1 usec

BIAS MEASUREMENT

Measurement Source: Receive Data

Measurement Range: 0 to 100% (0%=all zeros, 100%=all ones)

Measurement Accuracy: ± 1%

GRAPHS

Standard BERT Graph

Graphed Parameters: Bit Errors
Errored Blocks
Errored Seconds
Error Free Blocks
Error free Seconds
Sync Losse
Transmit BPVs (T1)
Receive BPVs (T1)
Transmit BPV Seconds (T1)
Receive BPV Seconds (T1)
Transmit BPV Free Seconds (T1)
Receive BPV Free Seconds (T1)

Vertical Scaling Factors (data): 10^0 through 10^5

Horizontal Scaling (time): 1 sec/div, 10 sec/div, 1 minute/div, 10 minutes/div, and 1 hour/div.

Table 1-1. Model 5500 Specifications (Cont.).

JITTER OPTIONS

Low Speed Jitter

Frequency Range:	75 bps to 72 Kbps
Accuracy:	± 1.0%
Measurements : (in percent of one bit time)	Positive Peak Jitter Negataive Peak Jitter Average Jitter Peak-to-Peak Jitter

High Speed Jitter

Available Frequencies:	1.544 Mbps (T1-J02 option) 2.048 Mbps (G.703 -J05 option)
Amplitude Range:	0 - 12.75 unit intervals, generator/ receiver
Modulation Range:	10 Hz - 40 KHz, generator/receiver
Available Masks:	AT&T CCITT

REMOTE CONTROL

Connection:	RS-232 Printer/Remote Control Interface IEEE-488 Bus Interface
Controllable Functions:	All Menu Selections Hexidecimal Keypad entries Front panel keys

Table 1-1. Model 5500 Specifications (Cont.).

DISPLAY

Type: High Resoultion, monochrome, cathode ray tube
Size 5 inch
Phosphor Green

Menus Displayed

Standard	BERT
	BERT Format
	Remote Configuration
	System Configuration
	User Programs
	Print Selection
	User Pattern
	Graph Display
	Graph Data Selection
	Big BERT
	Menu Matrix Help
Optional	MSU Configuration
	G.821 Parameters
	High Speed Jitter

POWER REQUIREMENTS

Voltage:	User Selectable: 90-130 volts ac or 180-250 volts ac
Frequency:	45 to 450 Hz
Power:	120 volt-amperes maximum

ENVIRONMENTAL

Operating Temperature:	0 degrees C to +50 degrees C
Storage Temperature:	-10 degrees C to +85 degrees C
Humidity:	90% non-condensing

PHYSICAL

5500

Height:	5.25 inches
Width:	17.20 inches
Length:	12.79 inches
Weight:	23 pounds

5500 Interface Module

Height:	1.75 inches
Width:	7.25 inches
Length:	8.5 inches
Weight:	3 pounds (average)

1.2 EQUIPMENT SUPPLIED

The Model 5500 is shipped with the following:

a. Instruction Book
b. Power Cord
c. Model 5500-200 RS-232 Interface Module

1.3 OPTIONS

Table 1-2 presents the options available for the Model 5500.

Table 1-2. Model 5500 Options.

MODEL	FUNCTION
Model 5500-200	RS-232 Interface Module
Model 5500-300	CCITT V.35 Interface Module
Model 5500-450	RS-449/MIL-188C-114 Interface Module
Model 5500-500	TTL Interface Module
Model 5500-538	DDS Interface Module
Model 5500-539	DSØ/DSØA Interface Module
Model 5500-555	MSU I/O Control Module
Model 5500-600	DS1/DS1C Interface Module
Model 5500-624	DS1 (T1) Interface Module
Model 5500-628	ESF (T1) Interface Module
Model 5500-700	T-2 Interface Module
Model 5500-805	CCITT G.703 8.448 Mbps Interface Module
Model 5500-810	CCITT G.703 64 Kbps Interface Module
Model 5500-815	CCITT G.703 2.048 Mbps Interface Module
Model 5500-828	CCITT G.703 2.028 Mbps Framed/Unframed Interface Module
Model 5500-900	Bell 303 Interface Module
Model 5500-J01	Low Speed Jitter
Model 5500-J02	High Speed (T1) Jitter
Model 5501	G.821 Performance Evaluation
5500-P01	Printer
5500-RK19	19" rack mount kit
5500-CLO1	Precision Clock Package - All internal clocks ±1ppm
5500-CLO2	Precision Clock Option -one oscillator-user selects ±1ppm
5500-DM01	12" CRT Display Monitor
5500-628-TP	Breakout cable for access to D4 and ESF signals.

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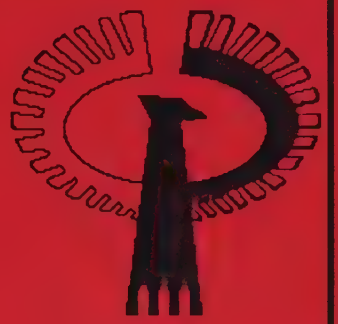
Data Communications Analyzer



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34-00015-022TB
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installation

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2.O GENERAL

This section contains information necessary for the correct installation of the Phoenix Model 5500 data communications analyzer. Included are initial inspection procedures, power and grounding requirements, and procedures for repackaging the instrument for shipment.

2.1 UNPACKING AND INSPECTION

The model 5500 is carefully packaged to prevent damage in shipment. Upon receipt carefully inspect the condition of the shipping container. If the container shows any evidence of damage, notify the carrier **before** continuing with the unpacking. Failure to notify the carrier of damage to the container before unpacking **may invalidate any claim for damages**. After unpacking the unit, retain the shipping container for future use. After unpacking, examine the exterior of the unit to insure it is free of scratches, dents, and any other visible sign of damage.

If the 5500 was damaged in shipment, file a claim with the carrier immediately. Check to insure you have received the supplied accessories (listed in paragraph 1.2 of this instruction book).

2.2 SAFETY SUMMARY

The following safety precautions must be observed whenever the 5500 is operated, serviced, or repaired. Failure to comply with these and other specific warnings and cautions within this instruction book is a violation of Phoenix microsystems' safety standards of design, manufacture, and intended use of the test set. Phoenix microsystems, inc. assumes no liability for the customer's or user's failure to comply with these precautions.

GROUNDING

The 5500 chassis and cabinet must be connected to an electrical ground for proper operation and to minimize shock hazard. The unit is furnished with a three conductor AC power cable which incorporates a ground lead. The power cable must be connected to an approved three contact electrical outlet or to a three conductor to two conductor adapter with a grounding wire (green) connected to electrical ground at the outlet.

EXPLOSIVE ATMOSPHERE

The 5500 must never be operated in the presence of any flammable gases or fumes. Power must not be applied to this or any instrument under such conditions due to the potential for explosion.

HIGH VOLTAGE CIRCUITS

Only qualified maintenance personnel should remove the instruments covers. Dangerous voltages may exist within the unit even after the power cable has been disconnected. Do not attempt to replace components with the power cable connected. To avoid possible serious injury

always disconnect the power and discharge circuits, particularly near the CRT, before touching any internal circuits or components.

SERVICE AND ADJUSTMENT

The 5500 contains few user serviceable parts. Internal service or adjustment should only be performed by Phoenix microsystems' repair personnel or authorized maintenance facilities to ensure that the safety features of the instrument are not compromised.

CATHODE RAY TUBE (CRT)

Use caution when handling the CRT. To avoid breakage of the CRT and the resulting implosion, do not jar or handle the 5500 in a rough manner while the internal circuitry is exposed. Removal, repair, or replacement of the CRT should only be done by qualified maintenance personnel.

LINE VOLTAGE

Before connecting the AC power cord make sure that the line voltage switch on the 5500 power supply module is set to match the source voltage.

FUSES

Always replace a blown fuse with an identical replacement fuse. **Never** use a fuse of a larger value or attempt to defeat or bypass the fuse.

ENVIRONMENTAL

Do not exceed the operating temperature limits (0 to 50 degrees C).

INTERFACE MODULES

Do not apply power to the 5500 without an interface module plugged into the unit. **Never** remove an interface module from or insert an interface module into the 5500 while the power is on. **Always** remove power first to prevent possible damage to the interface module and/or the 5500.

2.3 PRE-INSTALLATION CHECK

2.3.1 110/220 Volt Selection

The 5500 may be operated from any power source supplying 100 to 120 volts AC, 220 to 240 volts AC, 47 to 66 Hz, single phase.

> ***WARNING***
>
> Damage to the unit may result if the line voltage is not selected to match the input power source.

The 5500 is shipped from the factory preset for operation from a 110 VAC, 60Hz source. To operate the unit from a 220 VAC source, the following steps must be followed:

1. Locate the 5500 power supply module on the rear of the 5500 (refer to figure 3-2).

2. Locate the 110 VAC/220 VAC switch on the rear of the power supply module.

3. Place the 110 VAC / 220 VAC switch into the 220 VAC position.

The 5500 is now ready for operation from a 220-240 VAC, single phase source.

2.3.2 50/60 Hertz Selection

Upon initialization, the Model 5500 video frequency defaults to 60 hertz. The user may select either 50 or 60 hertz by pressing the 6 key on the keypad (for 60 hertz) or the 5 key on the keypad (for 50 hertz) at power up. This key must be the first key pressed after power up. After the key is pressed, the value is stored in non-volatile RAM and all future power ups will come up at the last chosen frequency.

2.3.3 5500 CRT Saver

Upon initialization the 5500 defaults to CRT saver OFF. The user may enable the CRT saver (which turns the CRT off 20 minutes after the last key was pressed) by pressing the 2 key on the keypad as the first key pressed after power up. After the key is pressed, the value is stored in non-volatile RAM and all future power ups will come up with CRT saver enabled. When enabled, after the screen has been turned off, depressing any key on the 5500 will re-enable the video for another 20 minutes.

2.3.4 Remote Printer Port Configuration

The 5500 RS-232 remote port is capable of connecting to either a DCE (Data Circuit-Terminating Equipment) type device or a DTE (Data Terminal Equipment). There are 6 selector (3 sets of 2) switches on the 5500 control board that must be configured to permit the 5500 to communicate with the device connected to the port.

> ***NOTE***
>
> A DTE deviced must be connected to a DCE device and vice-versa.

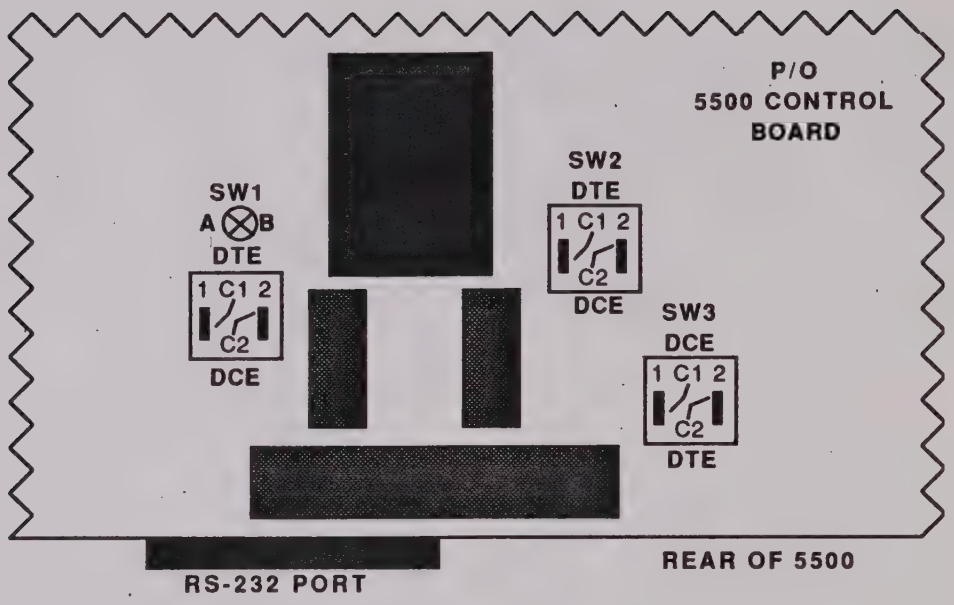
To gain access to these switches, the top cover of the 5500 must be removed. This is accomplished by removing the 2 screws holding the top rear retaining bezel, and athen sliding the top cover and bezel back to expose the 5500 control board.

The three sets of switches are mounted on the control board, near the RS-232 port, as shown in figure 2-1. Each switch has DCE and DTE indications printed on the board. If a data terminal equipment (DTE) device, such as a printer or CRT is connected to the RS-232 port, then set all the switches to DCE so the 5500 appears as a DCE device. Likewise, if a data circuit-terminating equipment (DCE) device, such as a modem, is connected to the RS-232 port, then all the switches must be set to DTE so the 5500 appears as a DTE device.

Table 2-1 lists the interface signals and their function for DCE and DTE with the corresponding pin assignments.

2.4 PACKAGING FOR SHIPMENT

Use the original packing material, if available, when packing the 5500 for shipment. If the original material is not available, package the 5500 to the current best commerical standards for electronic equipment. Phoenix microsystems, inc.'s customer service department can provide information and recommendations on packing materials to be used.



DCE - DTE Select Switches on 5500 Control Board
Figure 2-1

Table 2-1. Remote Port Pin Functions.

PIN	FUNCTION		SOURCE	
	DTE	DCE	DTE	DCE
2	TXD	TXD	5500	USER
3	RXD	RXD	USER	5500
4	RTS	RTS	5500	USER
5	CTS	CTS	USER	5500
6	DSR	DSR	USER	5500
7	Sig GND	Sig GND	------	------
8	DCD	DTR	USER	USER
20	DTR	------	5500	------

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3.0 INTRODUCTION

This section of this instruction book contains turn-on procedures, setup procedures, and general operating instructions for the Model 5500 Data Communications Analyzer. This section is written around the Model 5500 with the 5500-200 RS-232 Interface Module installed. If you have another interface module installed in your unit, refer to the applicable pages in the options section of this manual for those areas that do not agree with this section (ie., some menu displays are interface module dependent).

3.1 CONTROLS AND INDICATORS

Table 3-1 presents the front panel controls and indicators found on the Model 5500. Table 3-1 is keyed to figure 3-1 by index numbers. Table 3-2 presents the rear panel controls and connectors and is keyed to figure 3-2.

Table 3-1. Model 5500 Front Panel Controls and Indicators.

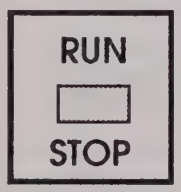
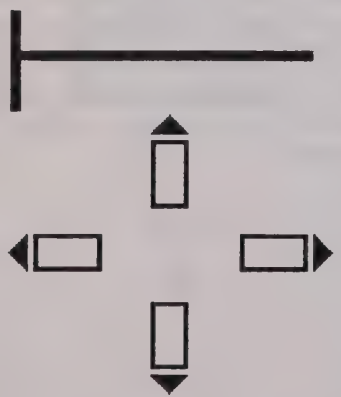
INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
1		RUN STOP	Controls 5500 operation. RUN led will be on when the 5500 is in the RUN mode.
2		MENU	These four keys are used to move around the matrix of the menus to bring the desired menu to the screen for viewing. These keys do not 'wrap-around'. If you have reached the limit of travel for a particular key, pressing that key will cause an audio tone to sound and the display will not change.

Table 3-1. Model 5500 Front Panel Controls and Indicators (Cont.).

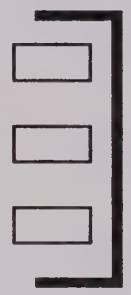
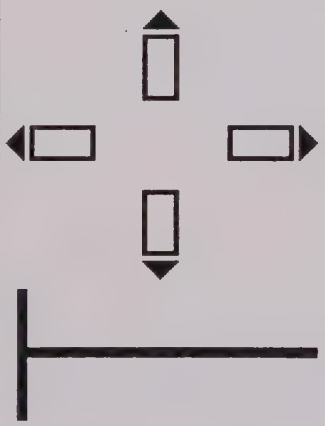
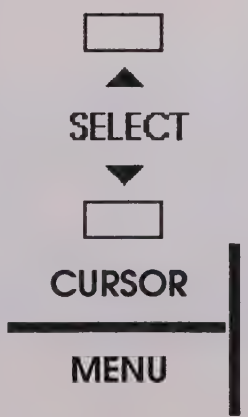
INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
3		*The mnemonic for these keys is software controlled and varies with each menu.*	These three keys are referred to as 'softkeys' since their function is controlled by the 5500 software as opposed to the hardware. Their function varies with the menu that is present on the display. The function of these softkeys will be explained with the individual menu descriptions.
4		CURSOR	These four keys are used to move the cursor around the menu. These keys do 'wrap around' allowing you to scroll through the cursor positions as many times as you desire. Generally, the cursor position is indicated by the selected item being displayed in the half intensity mode.
5		SELECT	After positioning the cursor over the desired parameter, the SELECT keys are used to scroll through (up/down) the parameter values to locate the desired selection.

Table 3-1. Model 5500 Front Panel Controls and Indicators (Cont.).

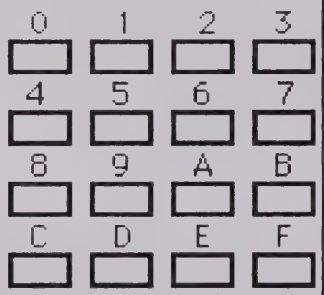
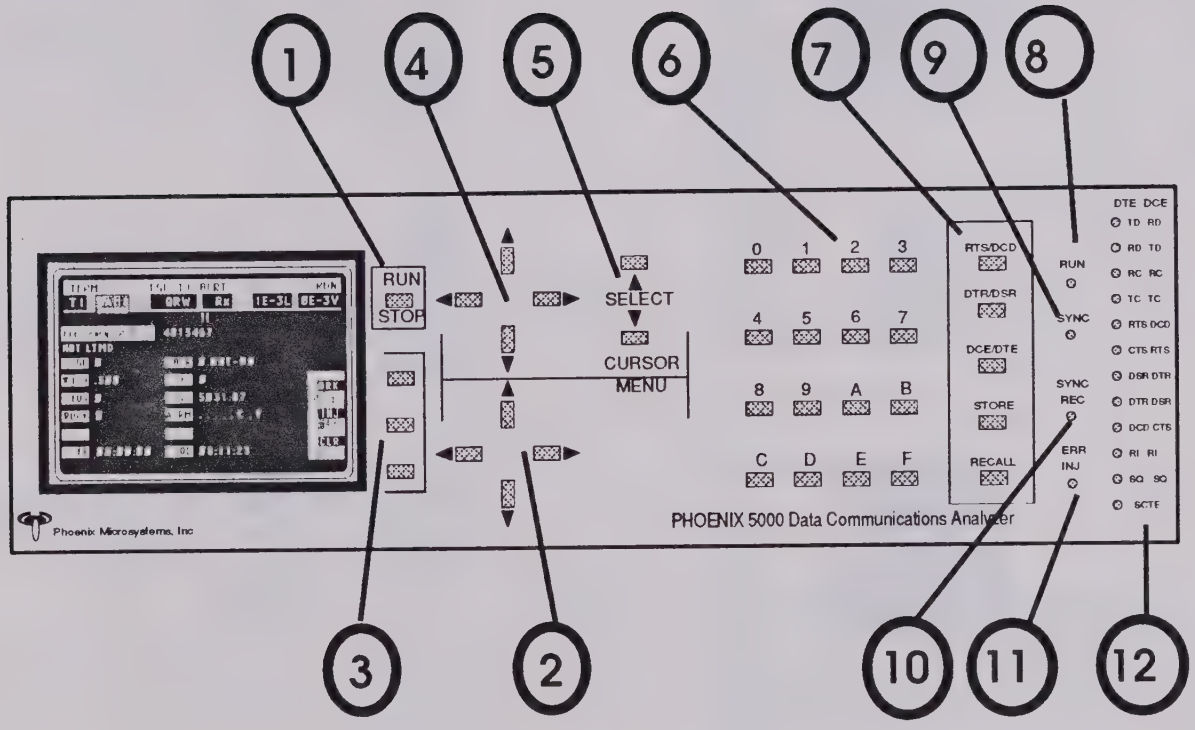
INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
6		*There is no mnemonic for the keypad.*	The hexidecimal keypad is used for data entry.
7		RTS/DCD	Toggles RTS in the DTE mode and DCD in the DCE mode.
		DTR/DSR	Toggles DTR in the DTE mode and DSR in the DCE mode.
		DTE/DCE	Selects DCE or DTE mode for the interface module.
		STORE	Stores the current test setup in selected memory location for recall.
		RECALL	Recalls a previously stored test setup from memory (press twice) or brings the Menu Matrix Help menu to the screen (press once).
8	RUN	RUN	This yellow LED is illuminated when the 5500 is in the run mode.

Table 3-1. Model 5500 Front Panel Controls and Indicators (Cont.).

INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
9	SYNC ●	SYNC	This yellow LED is illuminated when the 5500 is in synchronization with the incoming data stream.
10	SYNC REC ●	SYNC REC	This yellow LED is illuminated when the 5500 has recovered synchronization after having lost synchronization due to errors in the incoming data.
11	ERR INJ ●	ERR INJ	This yellow LED is illuminated whenever errors are being injected by the 5500 into the outgoing (transmit) data stream.
12	DTE DCE ● TD RD ● RD TD ● RC RC ● TC TC ● RTS DCD ● CTS RTS ● DSR DTR ● DTR DSR ● DCD CTS ● RI RI ● SQ SQ ● SCTE	*There is no mnemonic for the interface activity indicators*	These LEDs monitor the status of the interface connector lines and therefore are dependent upon the interface module installed.



Model 5500 Front Panel
Figure 3-1

Table 3-2. Model 5500 Rear Panel Controls, Connectors, and Test Points.

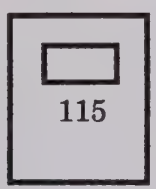
INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
1			Power cord connector for 5500. Before connecting main power be sure unit is set to match local power (refer to section 2 of this manual).
2			Main power fuse for 5500. A 2 amp, 250 volt, fast blow mini fuse. Always replace with a fuse of an identical current and voltage rating.
3			This is the main power switch for the 5500. The 1 position is 'ON' while the 0 position is 'OFF'.
4		**90-130VAC** **180-250VAC**	Main power select switch. Used to match the power module to the local source voltage. Switch is in the up position for input voltages between 90 to 130 VAC and in the bottom position for input voltages between 180 to 250 VAC.

Table 3-2. Model 5500 Rear Panel Controls, Connectors, and Test Points (Cont.).

INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
5			These test points provide several of the internal 5500 signals to the user. These signals may be used for any purpose. One of the common uses is to provide a trigger signal for an oscilliscope. These signals are all applied to the rear panel through TTL buffers. The following signals are available:
		TXD	Transmit data (data being transmitted by the 5500).
		TXC	Transmit clock
		XMIT PAT	Transmit pattern - pulse out that is synchronous with the beginning of the pattern and at the same repetition rate as the pattern.
		ERR	Error injection (signal each time an error is injected in the transmit data stream)
		SP	Spare test point - not used at this time.
		RXD	Receive data (data being received by 5500 receiver).

Table 3-2. Model 5500 Rear Panel Controls, Connectors, and Test Points (Cont.).

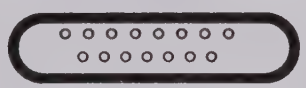
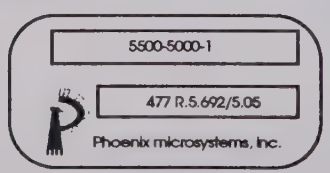
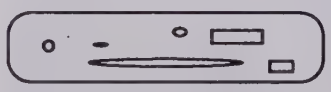
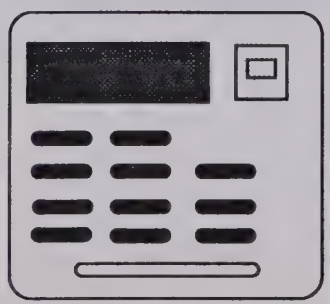
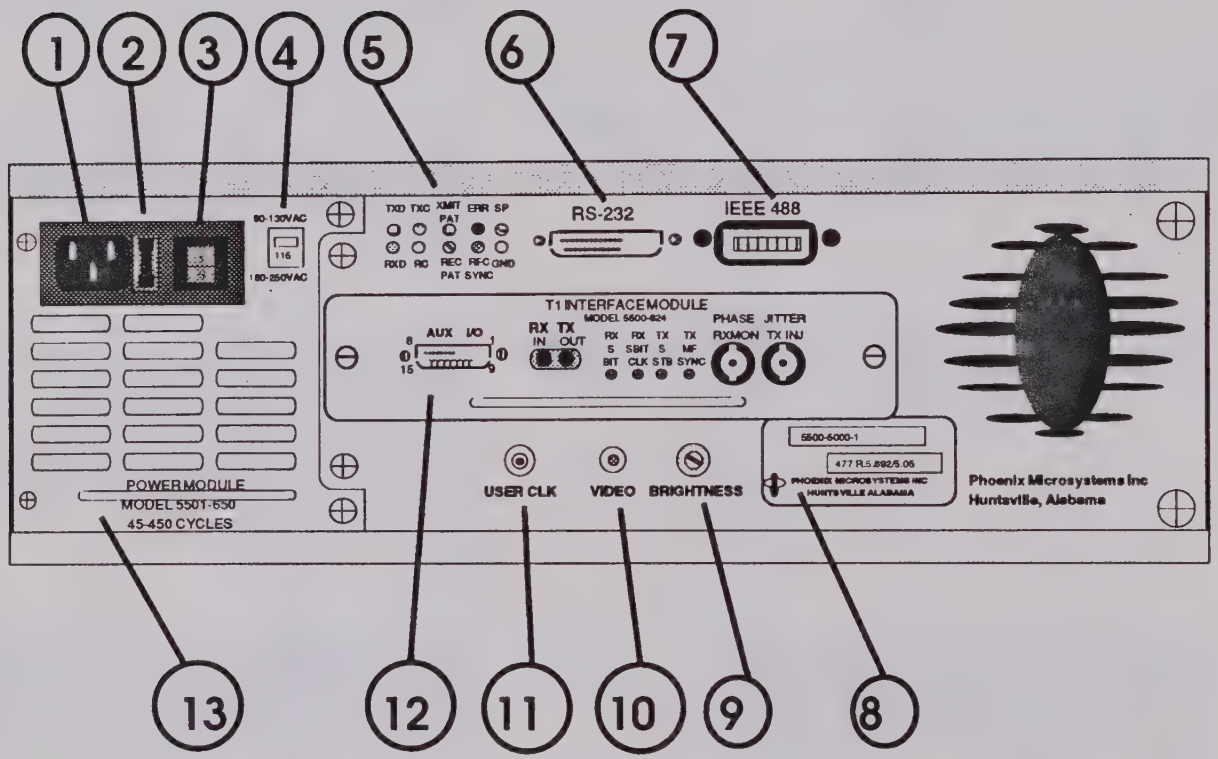
INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
5 Cont		RC	Receive clock
		REC PAT	Receive pattern sync - a pulse that is in synchronization with start of the pseudorandom receive pattern and is at the receive pattern repetition rate.
		REC SYNC	Recovered sync - an output pulse each time the 5500 recovers sync after having lost sync.
		GND	Signal ground.
6		RS-232	RS-232 interface port for connection of a printer for printing data/graphs or connection of a terminal for remote control operation.
7		IEEE-488	IEEE-488 port for connection of a controller for remote control operation.
8			Identification plate contains unit model number (5500-5000-1), serial number (477), hardware revision (5.692), and software revision (5.05).

Table 3-2. Model 5500 Rear Panel Controls, Connectors, and Test Points (Cont.).

INDEX NUMBER	CONTROL INDICATOR	MNEMONIC	FUNCTION
9		BRIGHTNESS	Control to adjust the intensity of the front panel CRT.
10		VIDEO	RS-170 composite video available at this jack to provide a video signal to an external monitor if desired.
11		USER CLK	The user may connect an external clock to this input connector. All functions of the 5500 will then be slaved to this external clock when external clock is selected on the setup menu.
12			Interface module which provides conversion between user protocol and the internal TTL logic used by the 5500. The options section of this instruction book provides complete information on the various interface modules available for the 5500.
13			Power module which provides the various DC voltages required to operate the 5500. The power module operates on 110VAC or 220VAC 50/60 hertz.



Model 5500 Rear Panel
Figure 3-2

3.3 INITIAL POWER UP

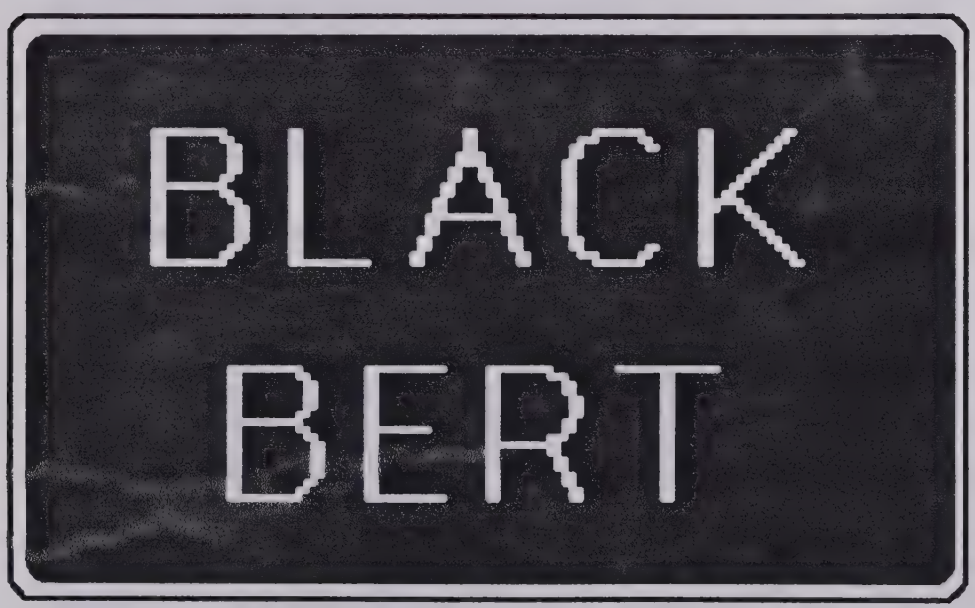
The following steps are provided for the first time user of the Model 5500. It provides information required to turn the Model 5500 on, select the desired menus, and how to make changes on the menus. Specific instructions for each menu follow this section.

1. With power removed, plug the desired interface module into the rear panel slot on the Model 5500 and secure with the two retaining screws.

2. Check the power select switch (refer to figure 3-2) to ensure the Model 5500 voltage is set to match the local source voltage.

3. Turn the power switch (refer to figure 3-2) to on.

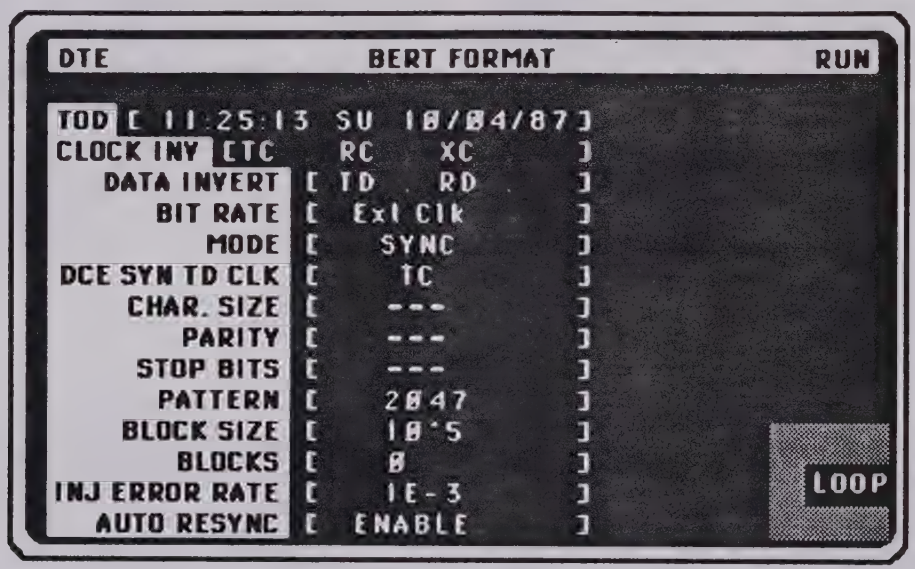
4. The first item to appear will be the Black BERT display, figure 3-3. If the 5500 was in the RUN state when it was last powered down, the Black BERT screen will appear only momentarily (about one second). If the 5500 was not in the RUN state when it was powered down, the Black BERT display will remain on the screen for about 30 seconds. In either case, pressing a menu direction key will bring the next screen to the display.



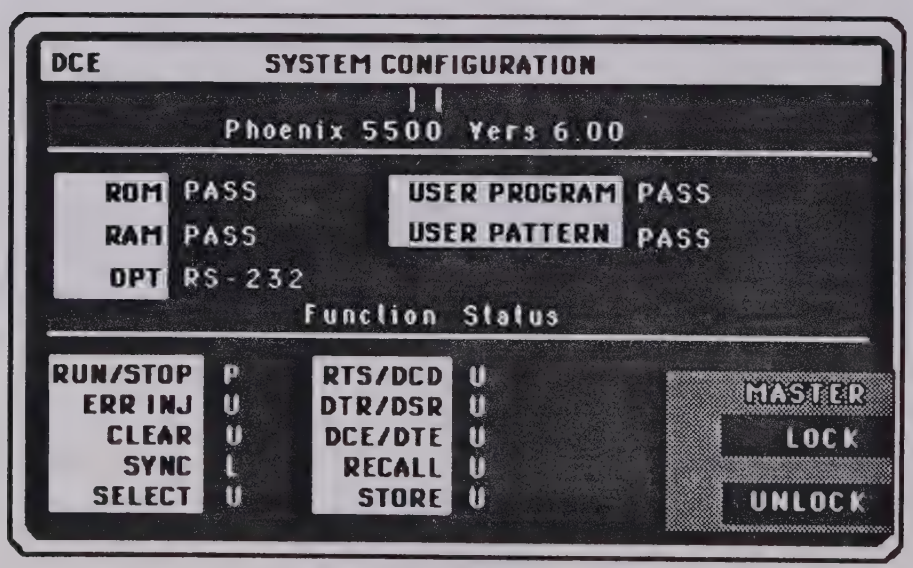
Black BERT Display
Figure 3-3

5. Following the Black BERT screen to the display will be either the BERT format screen (figure 3-4) or the System Configuration display (figure 3-5).

6. If the display is the System Configuration display (figure 3-5), It means that the 5500 has failed the self-test or that the USER PROGRAM or USER PATTERN displays have an error or have not been programmed. If the display indicates a ROM or RAM failure, return to step one and begin this procedure again. If the problem persists, return the unit to Phoenix microsystems, inc. for repair. If the USER PROGRAM or USER PATTERN indicate invalid, you may proceed with testing; however, the program/pattern stored in memory is suspect. This may be due to battery failure. In any case, do not use the stored pattern/program until it has been verified.


DTE
BERT FORMAT
RUN
TOD [11:25:13 SU 10/04/87]
CLOCK INV [TC RC XC]
DATA INVERT [TD RD]
BIT RATE [Ext Clk]
MODE [SYNC]
DCE SYN TD CLK [TC]
CHAR. SIZE [---]
PARITY [---]
STOP BITS [---]
PATTERN [2047]
BLOCK SIZE [10^5]
BLOCKS [0]
INJ ERROR RATE [1E-3]
AUTO RESYNC [ENABLE]
LOOP

RS-232 BERT Format Menu
Figure 3-4



System Configuration Display
Figure 3-5

7. At this time you will be able to determine if the Model 5500's 50/60 Hz selection has been set to match the local line voltage frequency. If the display is flickering/rolling and apears as if it has lost horizontal hold, the 50/60 Hz selection does not match the local line voltage frequency. To correct the problem, press the 6 key on the Hex keypad for 60 Hz operation or the 5 key for 50 Hz operation.

> ***NOTE***
>
> The 5 or 6 key must be the first key pressed after power up to change the frequency setting.

The Model 5500 is now ready to be used for testing. The following paragraphs will detail the various menus and how they are setup for testing.

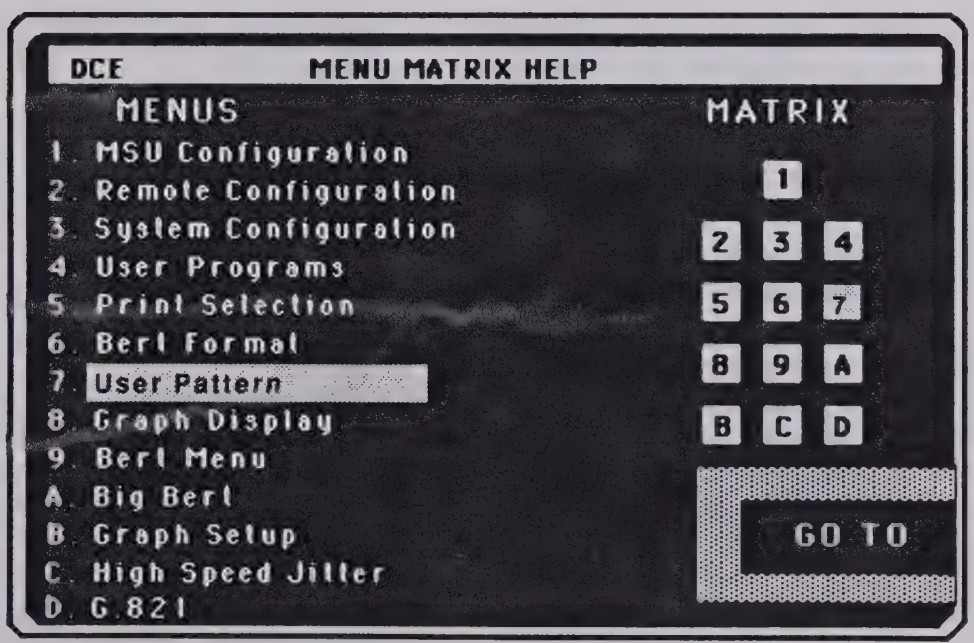
3.4 MENUS

The 5500 uses a series of menus, or displays, to provide the user with information and allow the flexibility which is needed in todays test equipment. In this section of the manual we will examine all the standard menus for RS-232 module and the differences in those menus when the Model 5500-628 ESF T1 module is inserted into the 5500.

3.4.1 Menu Matrix Help

The menu matrix help menu, figure 3-6, provides the user with a map of the menu matrix and a listing of all the menus. This menu remains essentially the same for all interface options. To use this menu, follow the steps below:

1. Press the **RECALL** key one time to bring the menu matrix help display to the screen.



Menu Matrix Help Display
Figure 3-6

2. The softkey for this menu is labeled **GO TO** on the menu and is the bottom key of the three softkeys on the front panel (refer to figure 3-1). Pressing this softkey brings to the screen the menu selected by the cursor. In figure 3-6, the cursor is shown over menu # 7, User Pattern and over the number 7 in the matrix. If the softkey were pressed in this example, the menu matrix help menu would be replaced by the User Pattern menu.

3. The cursor can be moved on this menu in one of two ways:

a. Pressing a number or letter on the keypad will move the cursor directly to that number in the matrix and the corresponding number on the list of menus.

b. Pressing the cursor direction keys moves the cursor within the matrix in the direction selected. The cursor within the list of menus follows the selection within the matrix.

The menu matrix help menu may be called to the screen by pressing the **RECALL** key one time.

3.4.2 BERT Format Menu

The BERT Format menu, located at position 6 in the matrix, is one of the most important menus in the operation of the 5500 as it is used to setup the majority of the test conditions. The menu is brought to the display by the following steps:

1. Perform the power up procedure in section 3.3 above.

2. Press the **RECALL** key one time to bring the menu matrix help screen to the display.

3. Press the **6** key on the keypad.

4. Press the GO TO softkey.

The BERT format menu, figure 3-7 or 3-8, should now be present on the screen.

3.4.2.1 RS-232 BERT Format Menu

The RS-232 BERT Format menus is illustrated in figure 3-7. The key line numbers correspond to the numbers below that explain each line of the menu. The softkey for this menu is the **LOOP** key which places the 5500 in the self-test loopback mode. Changes are made on this menu by moving the cursor over the desired parameter and then using the **CURSOR SELECT** keys to scroll the desired value under the cursor.

The lines on the BERT format menu are as follows:

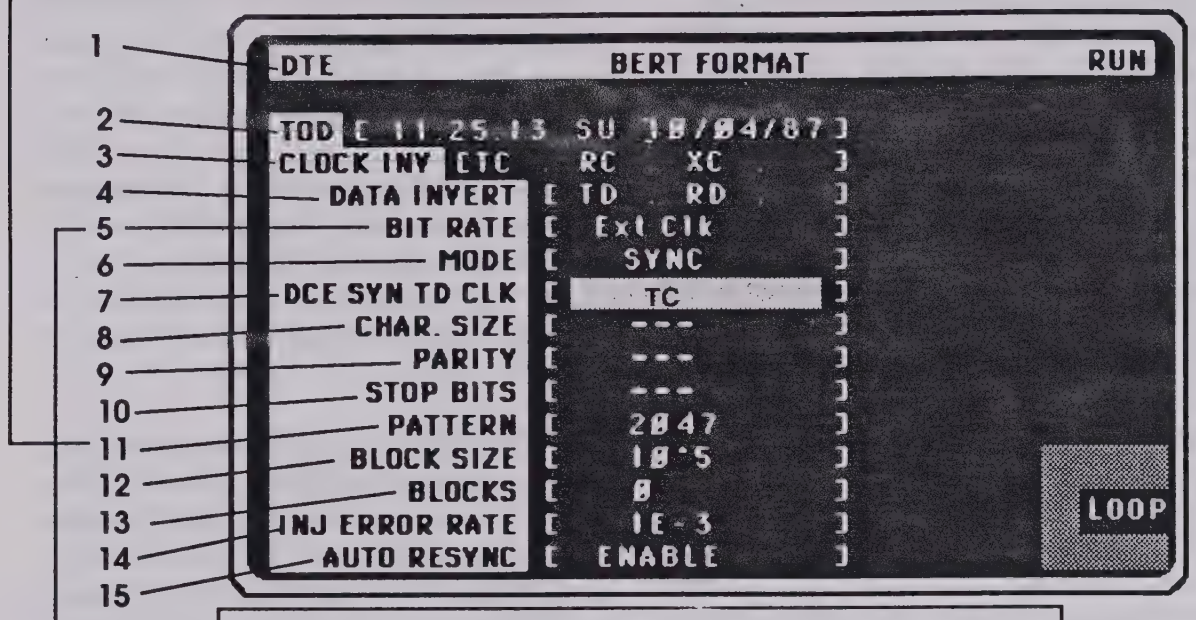
1. DTE/DCE - This section of the top line indicates what the 5500 is emulating, DTE or DCE.

2. TOD - This line contains the time of day and day/date/year. The correct time/date is set on this menu and once set, the information is retained in memory.

3. CLOCK INV - The user may elect to invert the polarity of the transmit (TC), receive (RC) or external (XC) clock signals. A dot (.) following the clock indicates the clock is NOT inverted. To invert the clock, place the cursor over the dot and press the CURSOR SELECT key. The dot will be replaced with an 'I' indicating that clock has been inverted.

PATTERNS AVAILABLE ON LINE 11

63, 511, 2047, REV 2047, (2^15)-1, (2^20)-1, QRW, T1 SET, T1 RESET, MARK, SPACE, ALT, FOX, SYSY 511, X25 511, USR1, USR2, USR3, USR4,



BIT RATES THAT MAY BE SELECTED ON LINE 5
(S) indicates data rate available in synchronous mode only.

BPS	Kbps		Mbps
75	14.4	144(S)	1.024(S)
110	16	153.6(S)	1.344(S)
134.5	19.2	168(S)	1.544(S)
150	24	192(S)	
200	28.8	224(S)	
300	32	230.4(S)	
600	48	256(S)	
1200	56(S)	288(S)	
1800	57.6(S)	336(S)	
2400	64(S)	384(S)	
3200	72(S)	448(S)	
3600	76.8(S)	460.8(S)	
4800	84(S)	512(S)	OTHER
6400	96(S)	576(S)	Opt Clk (S)
7200	112(S)	672(S)	Ext Clk (S)
8000	115.2(S)	768(S)	Usr Clk
9600	128(S)		

RS-232 BERT Format Menu
Figure 3-7

4. DATA INVERT - This line works in the same manner on the receive data (RD) and transmit data (TD) as the clock invert above.

5. BIT RATE - The internal bit rates which can be selected are listed in figure 3-7. The OPT CLK choice refers to the optional precision clock for specific frequency which the user may choose to purchase. The USER CLK choice refers to the rear panel clock input on the Model 5500. The user may input a frequency synthesizer to the USER CLK BNC connector and select any frequency from 75 bps to13 bps for operation.

6. MODE - The Model 5500 is capable of synchronous or asynchronous operation. Generally speaking, most systems operating at 2400 baud and above are synchronous with the exception of certain compressed bit rate voice systems. The Model 5500 can operate at bit rates up to 48 Kbps asynchronously.

7. DCE SYN TD CLK - (DCE mode synchronous transmit data clock) When the user selects DCE simulation operation of the Model 5500 it is necessary to then select whether the test set (simulating a MODEM) will supply clock (TC-Pin 15) to, or derive clock (XC-Pin 24) from the system under test in synchronous operation. If the user selects TC then the Model 5500 Transmitter's clock source is its own internal clock. If XC is chosen then the Model 5500 Transmitter derives its timing from the system under test. Note that this selection is only meaningful in synchronous DCE mode simulation and is primarily used only when operating at speeds greater than 1 Mhz.

8. CHAR SIZE - The number of data bits which make up a character in asynchronous data transmission is selectable from either the FORMAT or main BERT menus. Asynchronous character sizes of 5, 6, 7, or 8 bits length may be chosen. If CONTINUOUS is chosen then the Model 5500 sends out a continuous stream of data bits without start and stop characters. When operating in a synchronous mode there are no start and stop bits and so the bit stream is continuous or infinite and three dashes are displayed in the menu field.

9. PARITY - Parity bits in the data stream provide a means of error detection. In async data streams the user may select EVEN or ODD parity or may choose NO parity at all. Choosing EVEN parity means that the number of 1's in a data block must add up to an even number. Likewise ODD parity means the number of 1's in the block of data sums up to an odd number.

If, in EVEN parity, a block is received with three 1's in it, then the detector knows there has been at least one error. The choice of parity or no parity depends entirely on the system under test.

The parity bits are not used in synchronous data streams, therefore three dashes appear in parity field when the synchronous mode has been selected.

10. STOP BITS - Asynchronous, Byte oriented data transmissions employ start and stop bits to identify one byte from the next. A typical data transmission may be composed of a start bit, seven data bits, a parity bit and a stop bit. The choice of STOP BITS is either

1 or 2 and depends upon the system under test. This parameter has no meaning in synchronous transmission, and therefore the field contains three dashes.

11. PATTERN - The choice of pattern depends upon the test which the user desires to make. The Model 5500 uses industry standard pseudorandom sequences of various lengths for Bit Error Rate testing (refer to figure 3-7) plus a number of other patterns for specific uses as well as a USER programmable pattern up to 135 HEX characters long.

12. BLOCK SIZE - The number of bits which make up a block can be varied from 100 (10^2) to 1,000,000,000 (10^9). The choice of block size is a factor in the overall test length in bits since the block size times the number of blocks in the test equals a specific number of bits. The choice of block size may be dictated by any number of factors, such as the simulation of the actual signals, but in general the higher the bit rate, the larger the block size.

13. BLOCKS - The number of blocks in the test may be selected as any number from 1 to 9999. If a '0' is placed in this window, then the Model 5500 will run a test continuously until the **STOP** key is pressed. The user selects the BLOCKS by moving the half intensity marker to BLOCKS and setting in the desired number using the HEX keypad numbers.

14. INJ ERROR RATE - The Model 5500 enables the user to inject single or multiple bit errors at rates from 9x10-3 to 1x10-9 errors/bit. The user programs the error rate by scrolling the half intensity block over the INJ ERROR RATE field. The user must select the mantissa of the rate desired using either the **SELECT** keys or the HEX keypad. The choices are 0 to 9. A 0 (zero) will disable the error inject. Then the user must use the **CURSOR** key to move the block to the right and change the exponent from -3 to -9 as desired. Once set, the rate is retained in non-volatile memory. Error injection is most often used for identification and testing the integrity of a circuit.

16. AUTO RESYNC - The auto resync function in the Model 5500 has three states; enable, disable, and timed. When the auto resync feature is disabled, the 5500 will continue to count bit errors once synchronization has been obtained, regardless of the number of bit errors per unit time.

When the auto resync is enabled, the 5500 obtains synchronization and then continually monitors the bit error count and, when the bit error rate exceeds a predetermined threshold, the 5500 will declare it has lost synchronization and will not recover synchronization until a preset number of bits matches the pattern, usually set at 56 bits. During this time the 5500 is out of synchronization, error parameter collection is suspended, with only the time the unit is out of synchronization being accumulated.

In the timed resync mode, a number of 10 millisecond intervals (0-999, representing 0 to 9.99 seconds) is selected by the user as the time span of an internal timer. During the time cycle, if at least one bit error occurs during each 10 millisecond interval, the 5500 will count these errors until the timer runs out. When the timer runs out, the 5500 will check the bit error sync threshold to determine if sync should be broken. If

auto resync disable mode and restart the internal timer. During the timer period, two events are taking place; 1) the 5500 is continuing to accumulate bit errors and, 2) the 5500 is monitoring the data to determine if errors have ceased. If only one 10 millisecond interval is error free, the timer is reset. If errors have ceased, the 5500 continues and the timer is reset, awaiting the next bit error occurrence.

3.4.2.2 T1 BERT Format Menu

The T1 BERT Format menus is illustrated in figure 3-8. The key line numbers correspond to the numbers below that explain each line of the menu. There are three softkeys for this menu. The bottom softkey is the **LOOP** key which places the 5500 in the self-test loopback mode. The top two softkeys are used to select the appropriate termination mode; Bridge, Terminate, or Monitor using the following guidelines:

> ***NOTE***
>
> The top soft key is the **MON** key. Activate this key to the "highlighted" state for "MONITOR" mode. Deactivate the **MON** key to the "not highlighted" state to return to the highlighted BRDG or TERM mode. The middle softkey is an alternate function **TERM/BRDG** key. Activate this softkey to change from the displayed mode (i.e. TERM) to the alternate mode (i.e. BRDG).

BRDG mode (BRIDGE high impedance termination option; SAFEST for the curious when wishing to avoid interference with the monitored circuit).

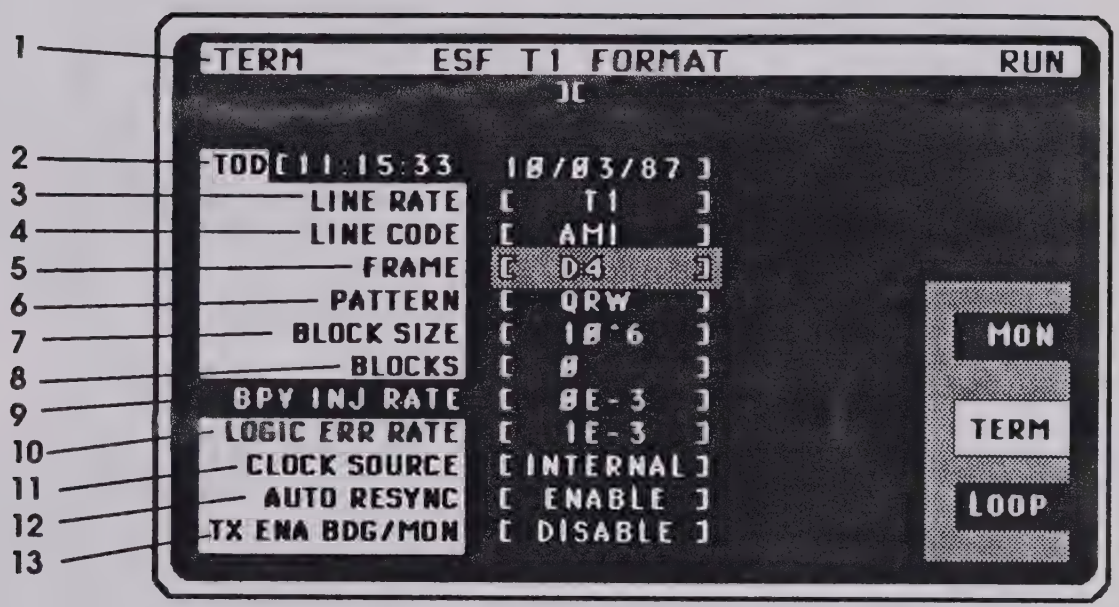
TERM mode (terminates the RX pair with 100 ohms -- to be used only when the monitored circuit "terminates" at the Model 628 test interface -- normally used only in out-of-service testing when the test set is substituted for the normal network terminating device).

MON mode (MONITOR mode is specifically for DSX panel test access via a standard DSX "MONITOR" jack which provides two 430 ohm resistors in series with tip and ring -- in this mode the test set will terminate the RX pair with 100 ohms, resulting in 20dB attenuation of the resistor isolated monitor signal. The resistors minimize circuit interference which might otherwise result from the test set load impedance, test probe contact bounce transients, or an improper test connection to a transmitter instead of a receiver.) The MONITOR mode envokes a 20dB amplifier (voltage gain of 10) to compensate for the 20dB attenuation of the 430 ohm resistors. The BRIDGE mode of termination is compatible with resistor isolated MONITOR jacks (by virtue of high impedance termination and 628 receiver amplitude tolerance); however, the MONITOR mode is more appropriate when remote test access requires test lead length in excess of fifteen feet. MONITOR jack remote test access wire lengths in excess of 2000 feet may be accommodated by using standard, Z0=100 ohm, wiring --with the 628 module in the MONITOR mode

Changes are made on this menu by moving the cursor over the desired parameter and then using the **CURSOR SELECT** keys to scroll the desired value under the cursor.

The following is a description of the lines on the T1 BERT format menu:

1. This line gives the status of the termination mode selected (TERM, BRDG, MON) with the softkeys as described above.



ESF T1 BERT Format Menu
Figure 3-8

2. TOD - This line contains the time of day and day/date/year. The correct time/date is set on this menu and once set, the information is retained in memory.

3. LINE RATE - This line shows the line rate for the interface module (in this case T1). There is no selection available on this line.

4. LINE CODE - This line is used to select the desired line code, AMI (alternate mark inversion) or B8ZS (bit eight zero suppression).

5. PATTERN - The choice of pattern depends upon the test which the user desires to make. The Model 5500 uses industry standard pseudorandom sequences of various lengths for Bit Error Rate testing (refer to figure 3-7) plus a number of other patterns for specific uses as well as a USER programmable pattern up to 135 HEX characters long.

6. FRAME - This line is used to select the framing format desired. Choices are SLC-96, ESF, D4, or DISABLE. The DISABLE selection would be made if it was desired to test unframed data at the T1 data rate.

7. BLOCK SIZE - The number of bits which make up a block can be varied from 100 (10^2) to 1,000,000,000 (10^9). The choice of block size is a factor in the overall test length in bits since the block size times the number of blocks in the test equals a specific number of bits. The choice of block size may be dictated by any number of factors, such as the simulation of the actual signals, but in general the higher the bit rate, the larger the block size.

8. BLOCKS - The number of blocks in the test may be selected as any number from 1 to 9999. If a '0' is placed in this window, then the Model 5500 will run a test continuously until the **STOP** key is pressed. The user selects the BLOCKS by moving the half intensity marker to BLOCKS and setting in the desired number using the HEX keypad numbers.

9. INJECT RATE - This line is a dual function line. The first choice the user has to make is the type of errors to be injected. This is accomplished by moving the cursor over the black area (where it says BPV INJ RATE in figure 3-8) on the menu. The user then may select from the following; BPV INJ RATE, F BIT INJ RATE, S BIT INJ RATE, CRC INJ RATE, or D INJ(CRCrate).

> ***NOTE***
>
> The available inject modes are automatically restricted to those appropriate for the selected combination of FRAME and CLOCK SOURCE modes (refer to table 3-3). Additional information on the inject modes can be found in the 5500-628 option instructions in the options section of this manual.

The second choice the user must make is selection of the inject error rate. The user programs the error rate by scrolling the half intensity block over the (----) INJ RATE value field. The user must select the mantissa of the rate desired using either the **SELECT** keys or the HEX keypad. The choices are 1 to 9. Then the user must use the **CURSOR** key to move the block to the right and change the exponent from -3 to -7 as desired.

Table 3-3. Error Injection Modes.

FRAME	CLK	BPV INJ	FBIT INJ	SBIT INJ	DATA INJ	CRC INJ
D4	IN	X	X	X		
D4	EXT	X	X	X		
D4	RX	X	X	X		
D4	THRU	X	X	X	X	
D4	JIT(JO2)	X	X	X		
D4	THRU-J(JO2)	X	X	X	X	
D4	THRU+J (JO2)	X	X	X	X	
SLC®96	INT	X	X			
SLC®96	EXT	X	X			
SLC®96	RX	X	X			
SLC®96	THRU	X	X		X	
SLC®96	JIT(JO2)	X	X			
SLC®96	THRU-J (JO2)	X	X		X	
SLC®96	THRU+J(JO2)	X	X		X	
ESF	INT	X	X		X	X
ESF	EXT	X	X		X	X
ESF	RX	X	X		X	X
ESF	THRU	X	X		X	X
ESF	JIT (JO2)	X	X		X	X
ESF	THRU-J (JO2)	X	X		X	X
ESF	THRU+J (JO2)	X	X		X	X
"UNFRAMED":						
DISABLE	INT	X				
DISABLE	EXT	X				
DISABLE	RX	X				
DISABLE	THRU	X			X	
DISABLE	JIT(JO2)	X				
DISABLE	THRU-J (JO2)	X			X	
DISABLE	THRU+J (JO2)	X			X	

10. LOGIC ERR RATE - The Model 5500 enables the user to inject single or multiple bit errors at rates from 9x10-3 to 1x10-9 errors/bit. The user programs the error rate by scrolling the half intensity block over the INJ ERROR RATE field. The user must select the mantissa of the rate desired using either the **SELECT** keys or the HEX keypad. The choices are 0 to 9. A 0 (zero) will disable the error inject. Then the user must use the **CURSOR** key to move the block to the right and change the exponent from -3 to -9 as desired. Once set, the rate is retained in non-

volatile memory. Error injection is most often used for identification and testing the integrity of a circuit.

11. CLOCK SOURCE - There are seven (four without the J02 jitter option) possible selections for the source of the transmit clock timing for the "TX OUTPUT" of the 5500-628 Module. These selections are; Rx, THRU, EXTERNAL, INTERNAL, **JIT, THRU-J,** and **THRU+J**. The clock sources listed in bold are only available with the J02 jitter option. Table 3-4 presents detailed information on each clock source.

12. AUTO RESYNC - The auto resync function in the model 5500 has three states; enable, disable, and timed. When the auto resync feature is dis-

Table 3-4. Clock Source Selections for ESF T1.

CLOCK SOURCE	DESCRIPTION
INTERNAL	Internal Oscillator (main chassis/not in module) Select INT CLK for any standalone equipment testing and anytime loop timing is not appropriate (someone in the network must originate the clock; everyone cannot slave to recovered clock).
Rx	"RX INPUT" recovered clock Select RX CLK anytime the "TX OUTPUT" is required to be "loop timed" to the "RX INPUT" clock.
EXTERNAL	TTL input via pins 15 (EXT CLK) and 36 (RETURN) of the 40 pin "TEST ACCESS I/O" connector. Connect any TTL external clock source @ 1544000+/-300 Hz for frequency tolerance testing of receivers, repeaters, etc. Connect any TTL precision clock, or network stratum 1 clock, etc., for use as: A) "TX OUTPUT" timing clock, and/or B) CSLP reference clock.
JIT	The JO2 OPTION modulates the internal clock source as specified via the Jitter Option Menu. The amplitude and frequency of phase modulation (and modulation wave shape - sine, triangle, or external modulation source) may be controlled to evaluate the jitter tolerance of network components.

Table 3-4. Clock Source Selections for ESF T1 (Cont.).

CLOCK SOURCE	DESCRIPTION
THRU	"RX INPUT" bit stream is retransmitted at "TX OUTPUT" with all data bits, frame bits, data link bits, bipolar violations, etc. unaltered. This mode may be used to provide an in line repeater function (ALBO phase compensation, clock recovery, & retransmission of a nominal 6Vpeak-to-peak signal with 10%-30% trailing edge overshoot per Pub 62411). This mode also provides for injection of data errors, frame errors, etc. in live traffic for evaluation of error tolerance of command/response protocols, error checking algorithms, packet switching protocols, etc. (when the standard BERT pseudorandom test patterns are inappropriate).
THRU-J	Same as "THRU" above except the phase jitter (up to 10 unit intervals peak-to-peak) of the recovered "RX INPUT" clock is attenuated by approx. 40dB at 120 Hz (and above) to a level of less than .1 unit intervals peak-to-peak. This de-jittered clock is then used as the "TX OUTPUT" clock source. This mode may be used to sectionalize jitter tolerance problems, especially when the standard BERT pseudorandom test patterns are inappropriate and/or when extended out of service testing and troubleshooting is not permitted.
THRU+J	Same as "THRU" and "THRU-J" above except the "jitter attenuated", recovered "RX INPUT" clock is phase modulated as specified via the JO2 jitter option menu, and then used as the "TX OUTPUT" clock source. This mode may be useful in characterizing the jitter tolerance margins (or shortcomings) of network components in "live traffic" situations.

abled, the 5500 will continue to count bit errors once synchronization has been obtained, regardless of the number of bit errors per unit time.

When the auto resync is enabled, the 5500 obtains synchronization and then continually monitors the bit error count and, when the bit error rate exceeds a predetermined threshold, the 5500 will declare it has lost synchronization and will not recover synchronization until a preset number of bits matches the pattern, usually set at 56 bits. During this time the 5500 is out of synchronization, error parameter collection is suspended, with only the time the unit is out of synchronization being accumulated.

synchronization being accumulated.

In the timed resync mode, a number of 10 millisecond intervals (0-999, representing 0 to 9.99 seconds) is selected by the user as the time span of an internal timer. During the time cycle, if at least one bit error occurs during each 10 millisecond interval, the 5500 will count these errors until the timer runs out. When the timer runs out, the 5500 will check the bit error sync threshold to determine if sync should be broken. If the 5500 breaks sync, it will enter the auto resync disable mode and restart the internal timer. During the timer period, two events are taking place; 1) the 5500 is continuing to accumulate bit errors and, 2) the 5500 is monitoring the data to determine if errors have ceased. If only one 10 millisecond interval is error free, the timer is reset. If errors have ceased, the 5500 continues and the timer is reset, awaiting the next bit error occurrence.

13. TX ENA BDG/MON -The TX OUTPUT jack is connected, tip and ring, to the secondary winding of the 628 transmitter output transformer via series relay contacts. The relay contacts are normally closed only in the "TERM" mode and open in the "BRDG" and "MON" modes (and open anytime "LOOP" is enabled). The "TX ENA BRDG/MON" ENABLE/DISABLE option allows the TX relay to be enabled or disabled in the Bridge and Monitor modes. The sleeve is connected to the test set "ground" circuit for shield termination.

3.4.3 BERT Menu

The primary purpose of the BERT menu is to view the results of a test, either as the test is running and/or when the test is completed. The 5500 monitors and keeps track of over 45 parameters simultaneously depending upon the interface module installed. To view the BERT menu, follow these steps:

1. Perform the initial power up procedure in paragraph 3.3.

2. Bring the menu matrix help menu to the screen as instructed in paragraph 3.4.1.

3. Press the 9 key on the keypad.

4. Press the GO TO softkey.

5. The BERT menu should now be on the display.

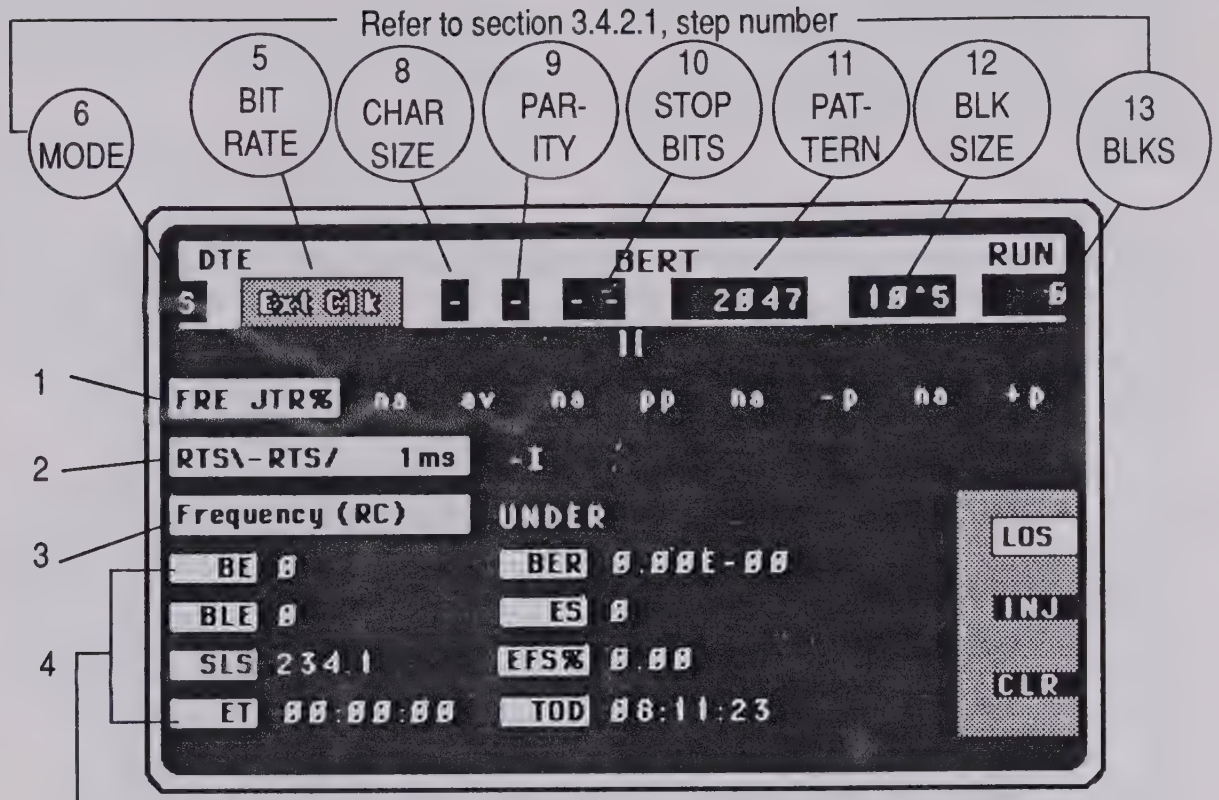
3.4.3.1 RS-232 BERT Menu

There are three softkeys for this menu. Their functions are as follows:

The top softkey (refer to figure 3-9) is a reflection of the SYNC and SYNC REC leds on the front panel. When the 5500 is in the RUN mode, the top softkey will display BRK until sync is acquired. When sync has been acquired, the SYNC led will turn on and the softkey will display SYNC. At this point in time, the softkey may be pressed to force a sync break if desired. If the 5500 looses sync, the SYNC led will turn off and the softkey will display LOS (loss of sync). When the 5500 recovers sync, the SYNC REC led and the SYNC led will be turned on and the softkey will display REC. At this time pressing the softkey will reset the SYNC REC led (turning it off) and change the softkey display to SYNC.

The second softkey (INJ) is used to turn the error injection on (INJ highlighted) or off (INJ as shown in figure 3-9).

The third softkey (CLR) is used to clear all the parameter counters and reset all the



PARAMETERS THAT MAY BE SELECTED FOR VIEWING					
BE	BER	BLK	BLE	EFB	EBR
TOD	MDY	ET	ED	ETS	ES
EFS	ESR	LOS	SLS	PF	ABE
ABER	CBE	CBER	EFS%	BITS	

RS-232 BERT Menu
Figure 3-9

will result in the display changing to '?'. This is to prevent accidental erasure of test data. To clear the parameters the user must press the softkey again before the question mark is replaced with CLR (about 2 seconds).

The top line of this display identifies the menu, shows if DTE or DCE has been selected, and if the 5500 is in the RUN mode. The second line is a condensed version of the BERT format menu discussed in section 3.4.2.1. The circled numbers in figure 3-9 refer to the step number in paragraph 3.4.2.1 that refers to that specific area of the display. The name of the display line is also included in each circle. By moving the cursor over any of these areas, it is possible to change that selected value just as if it were being accomplished on the BERT format menu. For example, if the cursor were located as shown in figure 3-9 (over Ext Clk), pressing the CURSOR SELECT keys would change the bit rate selection to one of the values shown in figure 3-7.

The remaining lines of the display are:

1. FRE JTR % - This line is only active when the J01, Low Speed Jitter option has been installed. Detailed information of the J01 option is found in the option section of this instruction book.

2. The measurement of the time interval between two specific events is required for some test applications. This line on the BERT menu permits the user to select the events from the following; TD (transmit data), RD (receive data), CTS, RTS, DCD, DSR, DTR, or SQ). The user may further select where the measurement is to take place; the leading or rising edge of the pulse (/) or the trailing or falling edge of the pulse (\). The time interval scale is the next item to set. This value is 1, 10, or 100 us, 1, 10, or 100 ms, or 1, 10, or 100 seconds. The numeric value in the field is then multiplied by the scale factor to obtain the time interval between the two events.

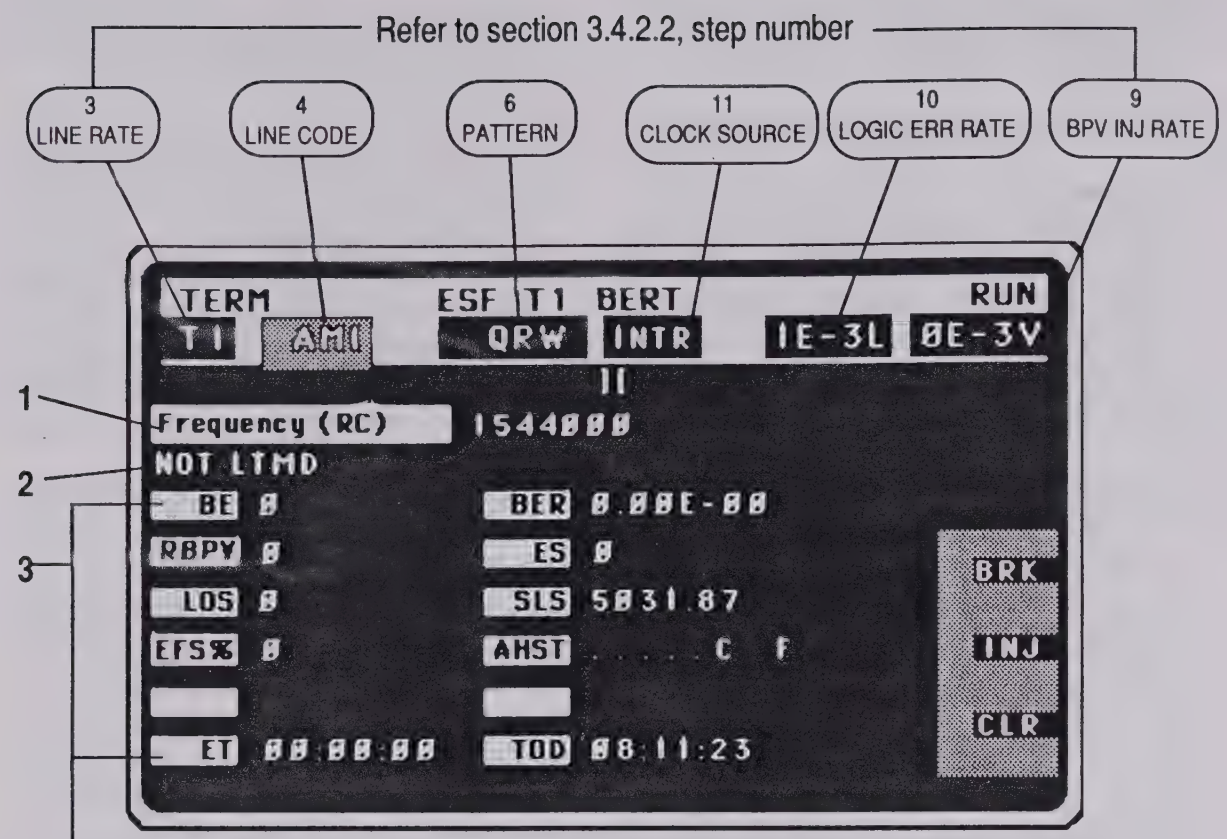
3. Frequency (RC) - This line is used to measure the frequency of reveive clock (RC), transmit clock (TC), external clock (XC), or the asynchronous bit rate (BR). The actual frequency being measured will appear in the field unless the frequency is below 150 Hz in which case the field will display UNDER.

4. There are eight windows available to the user to display any of the parameters listed in figure 3-9. The 5500 keeps track of all the parameters simultaneously and the user may scroll between any or all of them in these windows, at any time, without disrupting the test in progress.

3.4.3.2 ESF T1 BERT Menu

The three softkeys for this menu (refer to figure 3-10) perform the same functions as they do on the RS-232 BERT menu and are explained in paragraph 3.4.3.1.

The top line of this display identifies the menu, shows what termination mode has been selected, and if the 5500 is in the RUN mode. The second line is a condensed version of the ESF T1BERT format menu discussed in section 3.4.2.2. The circled numbers in figure 3-10 refer to the step number in paragraph 3.4.2.2 that refers to that specific area of the display. The name of the display line is also included in each circle. By moving the cursor over any of these areas, it is possible to change that selected value just as if it were being accomplished on the ESF T1BERT format menu. For example, if the cursor were located as shown



PARAMETERS THAT MAY BE SELECTED FOR VIEWING					
BE	BER	BLK	BLE	EFB	EBR
TOD	MDY	ET	ED	ETS	ES
EFS	ESR	LOS	SLS	PF	ABE
ABER	CBE	CBER	RBPV	RVR	RVS
RVFS	EFS%	%1sD	FLS	ALRM	AHST
FBE	FBER	FBES	FEFE	CRCE	CRER
CRES	CEFS	15Z	15ZS	FLOS	CSLP
WND+	WND-	BALS	YALS	BITS	

ESF T1 BERT Menu
Figure 3-10

in figure 3-10 (over AMI), pressing the CURSOR SELECT keys would change the LINE CODE selection to B8ZS.

The remaining lines of the display are:

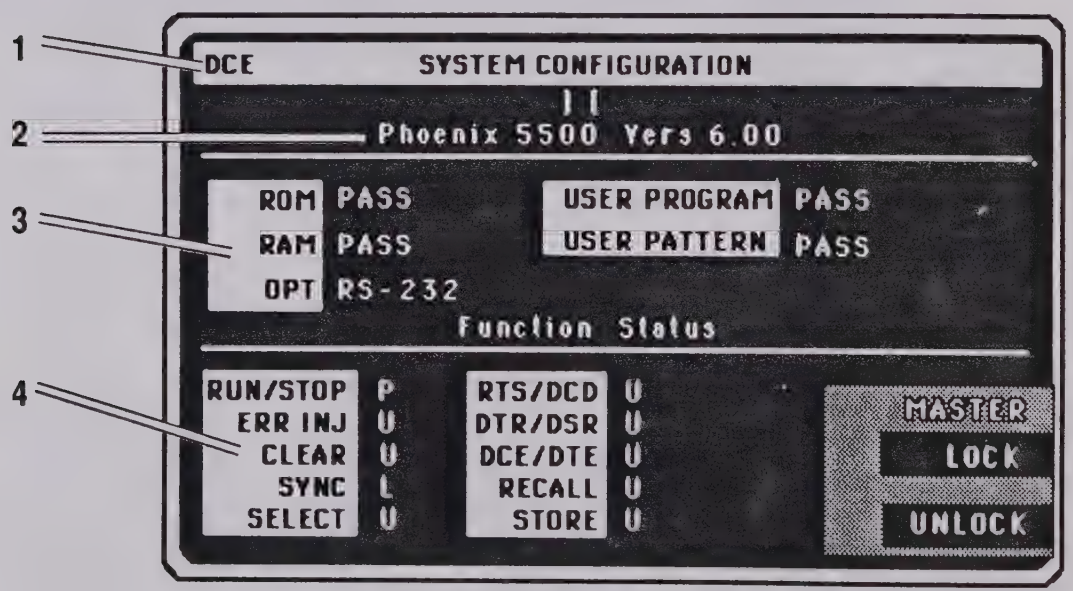
1. Frequency (RC) - This line is used to measure the frequency of reveive clock (RC), transmit clock (TC), or external clock (XC). The actual frequency being measured will appear in the field unless the frequency is below 150 Hz in which case the field will display UNDER.

2. This line is used in conjunction with the clock slip (CLSP) measurement. As long as CLSP remains within the range of plus or minus unit intervals, the LTMD (loop timed) indication will be displayed in this field. When CSLP exceeds this range, the flashing NOT LTMD (not loop timed) indication will appear in this field.

3. There are twelve windows available to the user to display any of the parameters listed in figure 3-10. The 5500 keeps track of all the parameters simultaneously and the user may scroll between any or all of them in these windows, at any time, without disrupting the test in progress.

3.4.4 System Configuration Menu

The System Configuration Menu, presented in figure 3-11 is used to view overall 5500 system operation and provide a method to lock various controls.



System Configuration Menu
Figure 3-11

The softkey for this menu is the master lock. When the LOCK softkey is pressed, all the front panel controls listed on this menu are disabled. When the UNLOCK softkey is pressed, it unlocks all the function keys on this menu that had been locked. It is always a good idea to press the UNLOCK softkey prior to setting up the 5500 to run any test. Failure to notice that one of the front panel keys has been locked out can cause the user to spend many needless hours agonizing over how to get the 5500 to perform a particular function.

The following explains the lines presented on the System Configuration Menu:

1. This line is the same as the top line on the BERT and BERT Format menus. This line will change with the various interface menus. It will reflect DCE/DTE or the termination status of the module (LOOP, BRDG, TERM).

2. This line will present the software revision of the Model 5500. The display shown has software version 6.0 installed.

3. This area of the display is used to present the results to the Model 5500 power up self-test. The ROM, RAM, USER PROGRAM, and USER PATTERN are checked. The OPT line lists the various interface options and/or jitter options that are installed.

4. This area of the display allows the user to set the status of the front panel controls on the 5500. By placing the cursor over the letter to the right of the control name, pressing the cursor select keys will scroll the letter from P to U to L. The L indicates the control is locked and pressing that key will have no effect. The U indicates the key is unlocked and pressing it will cause it to function in its normal manner. P is the protected status and prevents that key from being accessed from the remote terminal.

3.4.5 Print Selection Menu

The print selection menus, illustrated in figures 3-12 and 3-13, are used in conjunction with an optional printer to provide the user with time and date stamped hard copy of test results. The only difference between the RS-232 Print Selection Menus and the ESF T1 Print selection Menu, is the number of parameters available for printing and the conditions under which a printout can take place.

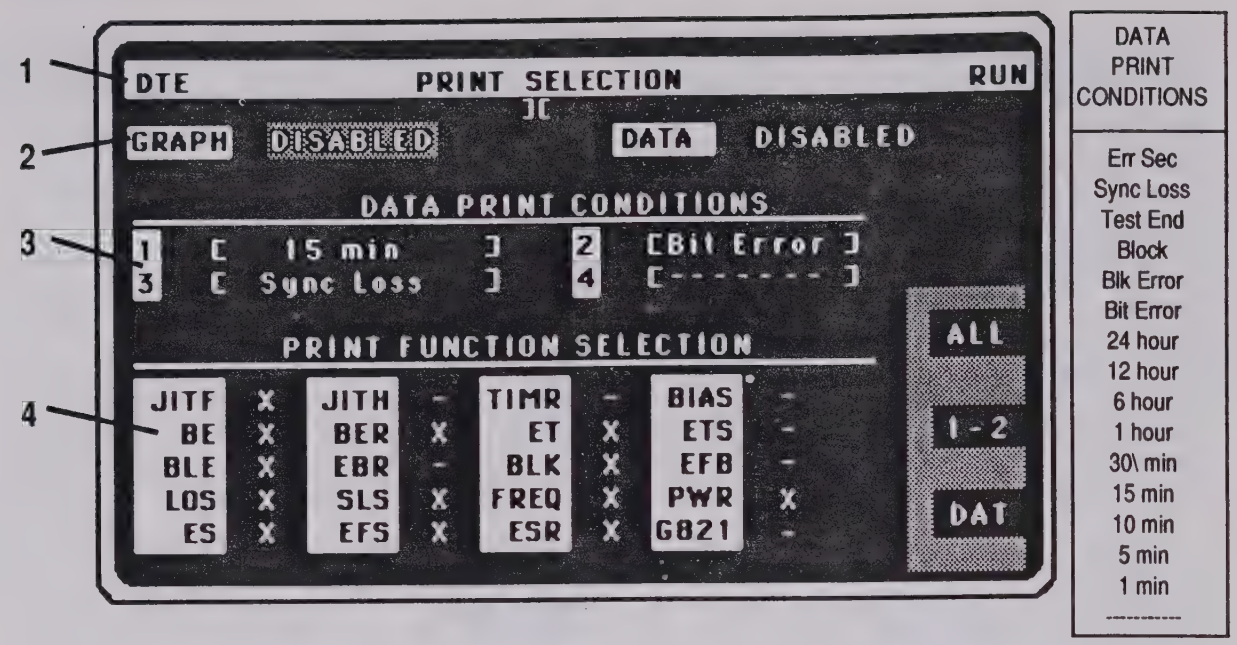
The softkeys for these menus are used to control what is to be printed. The top two keys, ALL and 1-2, are used when a graph is to be printed. Pressing the ALL softkey commands the printer to print the entire graph. Pressing the 1-2 softkey instructs the printer to print only that section of the graph that appears between cursor #1 and cursor #2 (see section 3.4.7 for information about the graph display). The final softkey, the DAT key, is used to instruct the printer to print the numeric data.

The explanation for each of the keyed areas in figures 3-12 and 3-13 follows:

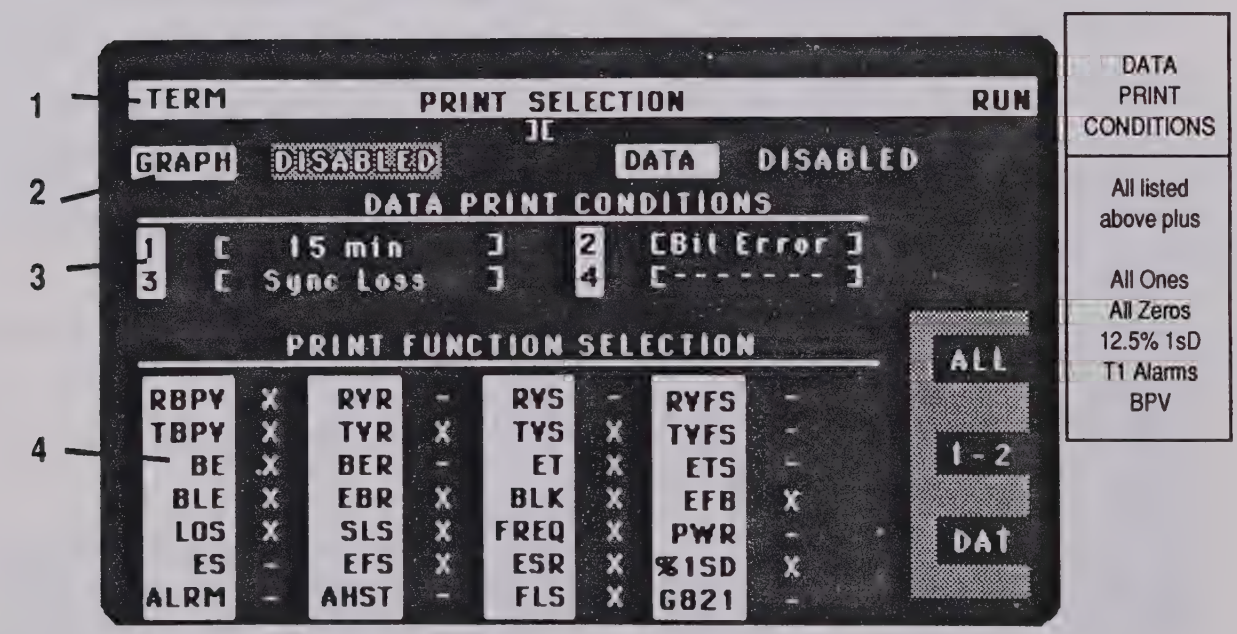
1. This line is the same as the previous menus.

2. This area of the display is used to ENABLE or DISABLE the graph and/or data printout functions. Place the cursor opposite the desired selection and use the CURSOR SELECT keys to select ENABLE or DISABALE.

3. This area of the menu, the DATA PRINT CONDITIONS, is used to select 1, 2, 3, or 4 conditions under which a print out will take place. In the example



RS-232 Print Select Menu
Figure 3-12



ESF T1 Print Select Menu
Figure 3-13

shown in figure 3-12, a printout will occur every 15 minutes (line 1), every time there is a bit error (line 2), and every time there is a sync loss (line 3). The available print conditions are listed in figures 3-12 and 3-13.

4. This area of the display, the PRINT FUNCTION SELECTION, is used to select those parameters the user wishes to have on the printed results. An "X" after the parameter indicates that that parameter has been selected to be printed. Selection is made by placing the cursor opposite the desired parameter, over the X or —, and using the CURSOR SELECT keys to enable (X) or disable (—) the printing of the parameter.

3.4.6 Graph Data Selection

The Graph Data Selection Menus, shown in figures 3-14 and 3-15 are identical except for the parameters available for graphing.

The softkeys for these menus are used to change the previous graph data selection to the current selection. The SELECT softkey will activate any changes that have been made on this menu and discard any stored graph data while the CANCEL softkey will cancel any changes that have been made without discarding the stored graph data. The softkey labels (SELECT and CANCEL) will flash to indicate that the stored configuration and the graph data do not match the displayed configuration.

The explanation for each of the keyed areas in figures 3-14 and 3-15 follows:

1. The top line of the display is the same as in previous menus.

2. The SAMPLE PERIOD field defines the sample resolution for the stored graph data. The resolutions available are 1 second, 10 seconds, 1 minute, 10 minutes, and 1 hour. Graph data can then be displayed at the selected period or the next 2 resolutions (selection is made on the Graph Display Menu, section 3.4.7).

3. The PRINT RESOLUTION field defines the resolution of the printed graph data. The graph can be printed at the sample period or the next two resolutions as summarized below:

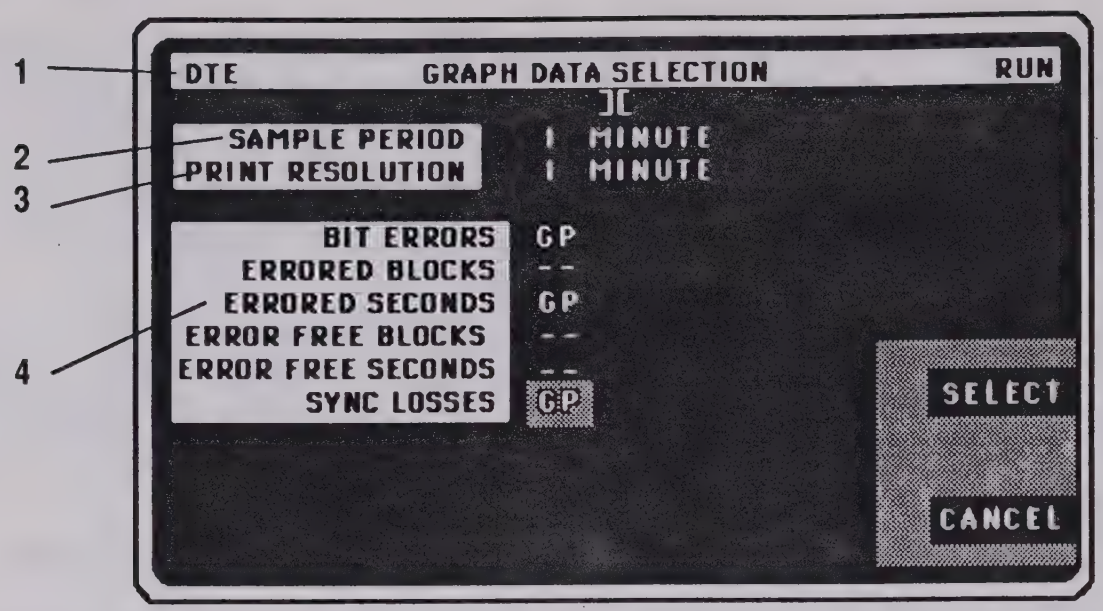
Sample Resolution	Print Period
1 second	1 or 10 seconds, 1 minute
10 seconds	10 seconds, 1 or 10 minutes
1 minute	1 or 10 minutes, 1 hour
10 minutes	10 minutes, 1 hour
1 hour	1 hour

4. The parameter field permits the user to select the parameter(s) to be graphed (G), graphed and printed (GP) or not selected for either (—). Selection is made by placing the cursor opposite the desired parameter and using the **CURSOR SELECT** keys to choose G, GP, or —.

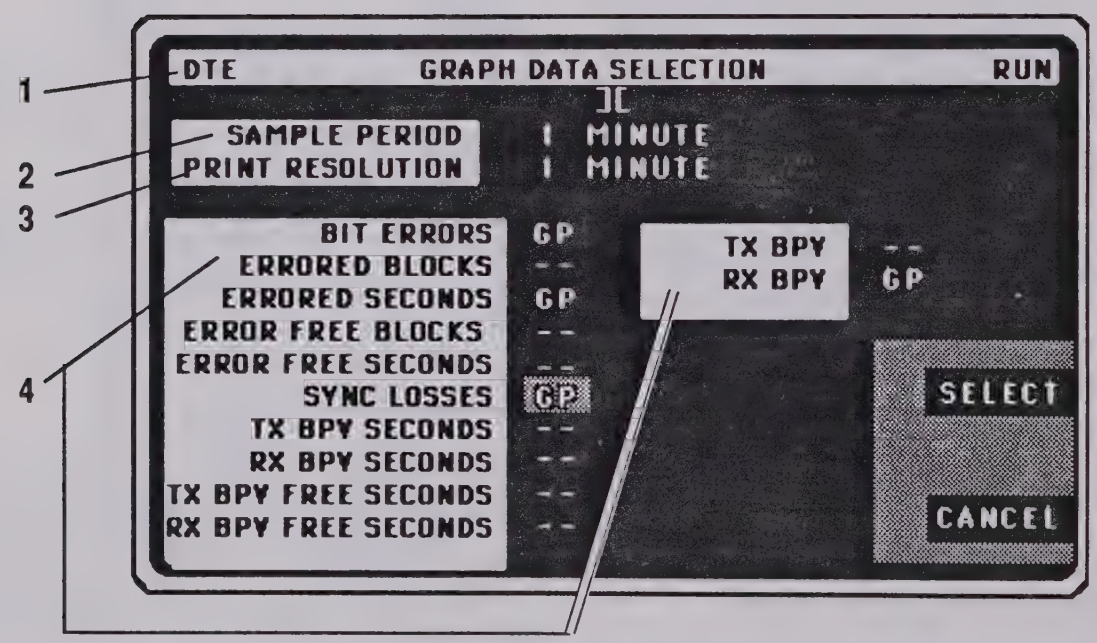
3.4.7 Graph Display

The Graph Display Menu, illustrated in figure 3-16, displays a single graph for any of the data types selected on the Graph Data Selection menu. This menu does not have any softkeys associated with the display.

The explanation for each of the keyed areas in figure 3-16 follows:

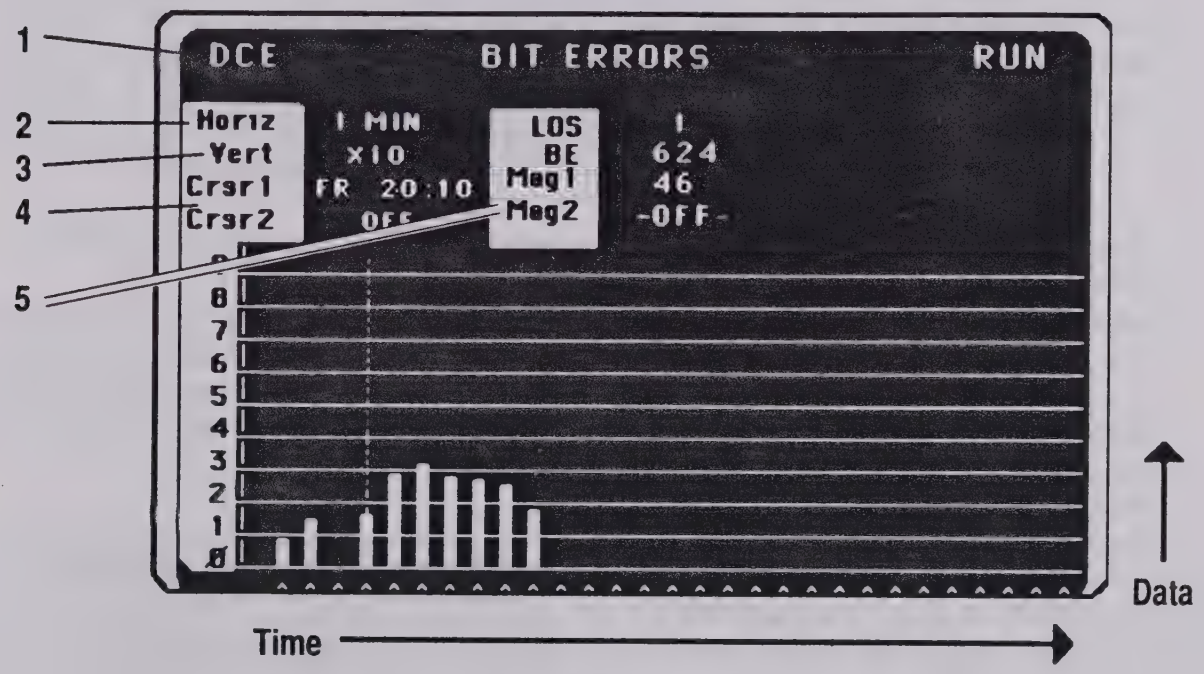


RS-232 Graph Data Selection Menu
Figure 3-14



ESF T1 Graph Data Selection Menu
Figure 3-15

Paramters That Can Be Viewed in Fields Above Mag 1	
WITH RS-232 MODULE INSTALLED BITS EFS% CBER CBE ABER ABE PF SLS LOS ESR EFS ES ETS ED ET MDY TOD EBR EFB BLE BLK BER BE	WITH ESF T1 MODULE INSTALLED ALL OF THE PARAMETERS LISTED ON LEFT PLUS YALS BALS WND- WND+ CSLP FLOS 15ZS 15Z CEFS CRES CRER CRCE FEFS FBES FBER FBE AHST ALRM FLS %1sD RVFS RVS RVR RBPV



Graph Display Menu
Figure 3-16

1. The top line of this display is different in that the title of the menu does not appear in the top center. Instead, the top center of this menu is used to display the parameter being graphed from the the list of those selected on the Graph Data Selection menu. The choice of which parameter to view is made by positioning the cursor over the function displayed at the top of the display and then use the **CURSOR SELECT** keys to scroll to the desired parameter. The remainder of the top line of this display is the same as the previous displays.

2. The Horiz field is used to select the time scale factor based upon the SAMPLE PERIOD selection made on the Graph Data Selection menu.

> ***NOTE***
>
> The graph data buffer is approximately 5400 samples long. Data is collected and stored until the buffer is full and then the oldest sample(s) are discarded as required to make room for new samples. The period of time that is represented by data in the buffer is a function of the sample period and the number of data types to be sampled. For example, assume a sample period of 10 seconds with three data types selected. To compute buffer length:
>
> Buffer length = (5400/3)*10 = 18,000 seconds = 5 hours

3. The Vert field selects the vertical resolution for the displayed graph. The vertical resolution selects a magnitude multiplier corresponding to the labels on the left side of the display.

4. The Crsr 1 and Crsr 2 define the day-of-the-week, hour, and minute of the samples at cursors 1 and 2. The two cursors may be used to print a section of the graph data. Cursor 2 may be off; if not, cursor 1 always precedes cursor 2.

5. The Mag 1 and Mag 2 fields display the magnitude of the data at cursors 1 and 2.

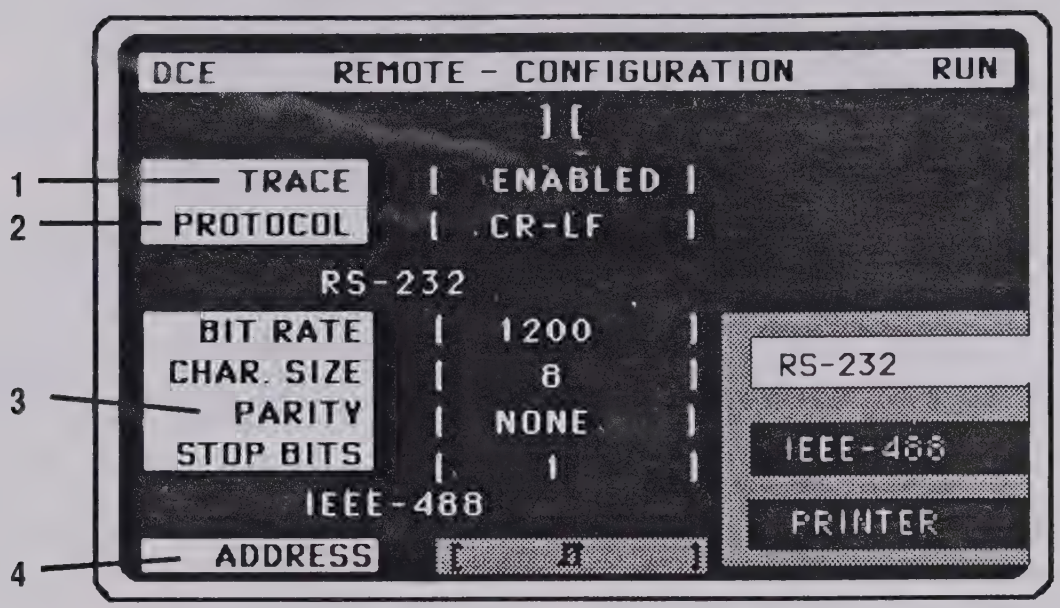
6. The two fields above the Mag 1 field are used to display the numeric results of a selected parameter (these parameters are not controlled by the parameters on the Graph Data Selection menu). To select the desired parameter, move the cursor to either field and use the **CURSOR SELECT** keys to select the desired parameter. The parameters available are listed in figure 3-16.

3.4.8 Remote Configuration Menu

The Remote Configuration Menu, illustrated in figure 3-17, is used to configure the 5500 remote port to match the device to be connected to the port, ie., a printer or terminal.

The softkeys for this menu are used to select RS-232, IEEE-488, or PRINTER. If RS-232 operation is going to be used, the user presses the RS-232 softkey if a terminal or modem is to be connected to the 5500 RS-232 remote port. If a direct printer connection is to be made via the RS-232 remote port, the PRINTER softkey is pressed. When the parallel IEEE-488 (sometimes refered to as GPIB or HPIB) remote port is to be used, the IEEE-488 softkey is pressed.

The explanation for each of the keyed areas in figure 3-17 follows:



Remote Configuration Menu
Figure 3-17

1. The TRACE field is used to view the character stream between the 5500 and the remote device over the remote port for possible troubleshooting. When the TRACE is ENABLED, the user will observe the data stream going to the remote device on the right half of the line and the data stream coming from the remote device on the left side of this line of the display. The trace will also be visible on all the other menus that have the trace brackets "][" on the second line of the display.

2. The PROTOCOL field is used to select the controller response format. The choices are CR-LF and ACK-NAK.

3. This area of the menu is used to select the various RS-232 protocols. The bit rate is selectable from 50, 75, 110, 150, 300, 600, 1200, 2400, 4800, 7200, or 9600 bps. The character size may be 7 or 8 bits, parity of odd, even, or none, and stop bits of 1, 1.5, or 2. These are all selected by placing the cursor over the selected field and using the **CURSOR SELECT** keys to scroll to the desired value.

4. The IEEE-488 bus enables the simultaneous connection of up to 31 devices to a single controller. Each device on the bus has a numeric address (0 - 30). It is therefore necessary to "tell" the 5500

what it's address is so that it will respond to information sent to it. This line is used to set that address into the 5500. Place the cursor over the address field and use the front panel keypad to enter the address.

3.4.9 User Program Menu

The User Program menu, illustrated in figure 3-18, is used to store up to ten complete configuration setups thus making it much faster to repeat a recurring test at a later date.

The softkeys for this menu are used to store (STR), recall (RCL), or clear (CLR) a program area. The STR softkey stores the current setup in the memory location indicated by the cursor. The RCL softkey recalls the setup configuration stored in the memory location indicated by the cursor. The CLR softkey clears the program name from the menu field for the selected memory location but does not clear the memory location of the configuration setup.

The front panel **STORE** and **RECALL** keys work in the same manner as the softkeys on this menu. To store a configuration into memory, follow these simple steps:

a. Setup the Model 5500 for the test desired.

b. Press the **STORE** key.

c. Press the keypad number for the memory location into which this setup is to be stored. (The user may overwrite any previously stored configuration by simply storing a new configuration in the old location.)

d. Name the program following the procedure in #1 below.

To recall a program, follow these steps:

a. Press the **RECALL** key twice within 2 seconds.

b. Enter the number of the desired program using the front panel keypad.

The explanation for each of the keyed areas in figure 3-18 follows:

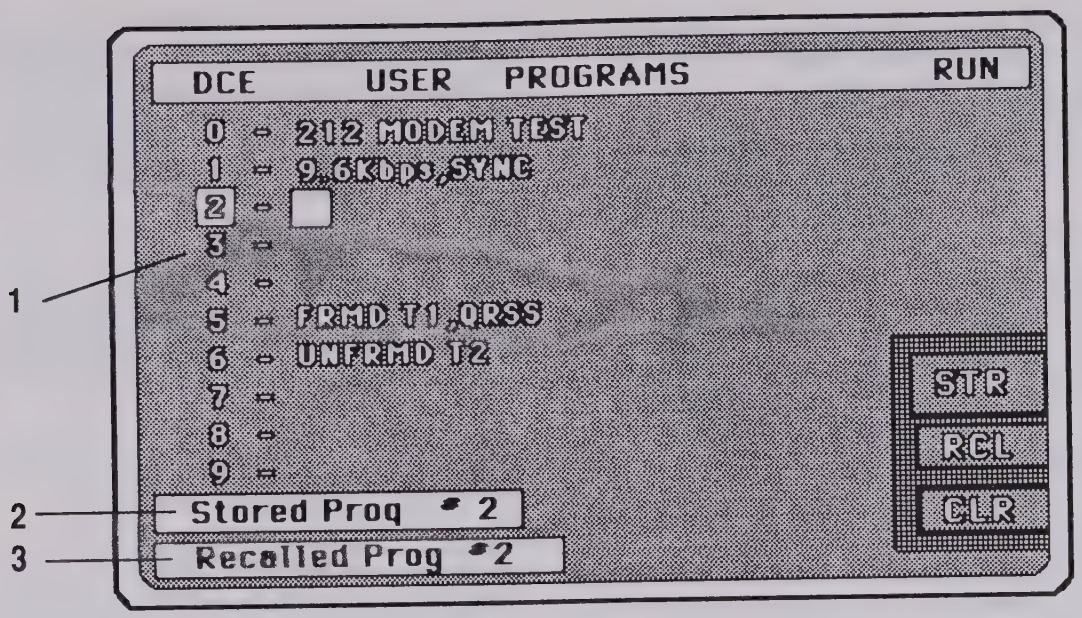
1. The fields numbered 0 - 9 represent memory locations in which a particular configuration setup may be stored by the user. The field opposite the number is provided so that the user may assign a name to the program for ease in identification. The name may be typed in using a terminal or by placing the cursor over the character position and then use the CURSOR SELECT keys to scroll through the character set until the desired character is in place.

2. The Stored Prog field displays the number of the most recent program stored by the user.

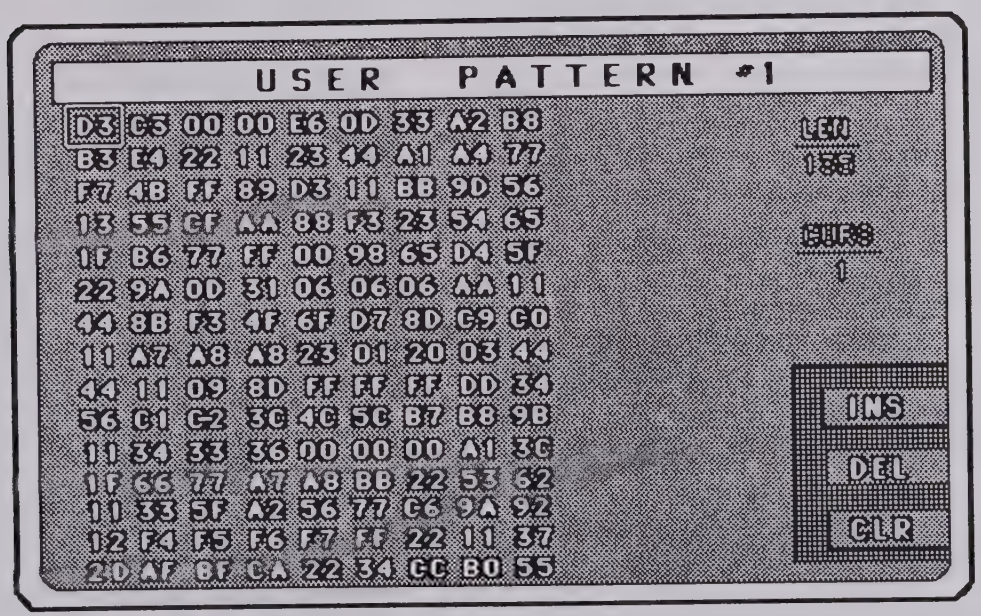
3. The Recalled Prog field displays the number of the most recent program recalled by the user.

3.4.10 User Pattern Menu

The USER PATTERN display, figure 3-19, allows the user to construct patterns for transmission by the Model 5500. The USER PATTERN selection, when chosen, causes the Model 5500 to transmit a repetitive pattern of whatever the operator has placed in the USER PATTERN display. The user is permitted to enter up to 135 characters (2048 in User pattern 4) in HEX from the front panel HEX keypad or over the remote control ports. Each character in HEX is an 8 bit long word so the total bit



User Program Menu
Figure 3-18



User Pattern Menu
Figure 3-19

length which could be input is 1080 bits. However, the user may enter as few as three characters if desired.

> ***NOTE***
>
> If the RAM backup battery failed or has been replaced it is possible that the Model 5500 will, power up, default to the system menu and flash the USER PATTERN memory block. This "error" can be ignored or the user may choose to place three or four characters into the User Pattern display. These can be any HEX characters or the user may want to place an actual pattern into memory.

Placing a HEX pattern into a memory is a straight forward process. The user scrolls to the USER PATTERN display using the MENU keys. Then, beginning in the upper left hand corner, enters the desired HEX character from the HEX keypad. Using the right CURSOR key, advance the half intensity block to the next position and enter another character. Repeat this process for the pattern length desired.

The user may desire to input a pattern on a binary, bit by bit basis. This is a somewhat more complex procedure, but the following table and examples will serve to explain the procedure.

Table 3-5 contains the 256 possible HEX combinations and their binary equivalents.

Step 1: Write the pattern desired bit by bit in the following format with the first transmitted bit first. An example T1 set code pattern is shown below (a continual repeating 10000).

1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 ----------

Step 2: Table 3-5 is constructed so that the least significant bit (LSB) is the inverse of what normally would be expected. This is a reference to allow the user to easily "invert" the desired pattern.

Step 3: Segment the pattern into 8 bit bytes as shown below until the pattern repeats. Note that in this example the pattern repeats after the fortieth bit.

10000100 00100001 00001000
01000010 00010000 10000100

Step 4: Compare the first byte (10000100) to the various bytes in the Table 3-2 and note that it is identical to the pattern for the HEX character set "21".

Step 5: Compare the second byte (00100001) to the tabulated values and note that it is equivalent to HEX "84".

Step 6: Repeat the procedure for all the remaining bytes. Note: that the 40 bit long pattern equates to the HEX character string "21 84 10 42 08".

STEP 7: The repetitive 10000 pattern has thus been converted into its HEX pattern "21 84 10 42 08" into the USER PATTERN display and the pattern generated will be a continuous 1000010000----.

> ***NOTE***
>
> This sample pattern (10000) is the Set Code used to loop back a T-1 Channel Service Unit (CSU) such as the Phoenix Model 1544.

An example of another use is a pattern with a long string of 0's to stress test a regenerative repeater's clock recovery and reshaping capability. Let us assume that the user desires a string of 31 0's. It is necessary to have at least one "1" in the string so the pattern would look like:

10000000 00000000 00000000 00000000 100

HEX 1 HEX 0 HEX 0 HEX 0

The user would enter the pattern in HEX as "10 00" and this would give a 31 zero transmission followed by a 1 and another string of 31 zeroes and so on.

With practice the user can input almost any binary pattern desired. The only restriction being the pattern must be able to repeat within 2048 bytes.

Table 3-5. Hex to Binary Conversion.

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
00	00000000	50	00001010	A0	00000101
01	10000000	51	10001010	A1	10000101
02	01000000	52	01001010	A2	01000101
03	11000000	53	11001010	A3	11000101
04	00100000	54	00101010	A4	00100101
05	10100000	55	10101010	A5	10100101
06	01100000	56	01101010	A6	01100101
07	11100000	57	11101010	A7	11100101
08	00010000	58	00011010	A8	00010101
09	10010000	59	10011010	A9	10010101
0A	01010000	5A	01011010	AA	01010101
0B	11010000	5B	11011010	AB	11010101
0C	00110000	5C	00111010	AC	00110101
0D	10110000	5D	10111010	AD	10110101
0E	01110000	5E	01111010	AE	01110101
0F	11110000	5F	11111010	AF	11110101
10	00001000	60	00000110	B0	00001101
11	10001000	61	10000110	B1	10001101
12	01001000	62	01000110	B2	01001101
13	11001000	63	11000110	B3	11001101
14	00101000	64	00100110	B4	00101101
15	10101000	65	10100110	B5	10101101
16	01101000	66	01100110	B6	01101101
17	11101000	67	11100110	B7	11101101
18	00011000	68	00010110	B8	00011101
19	10011000	69	10010110	B9	10011101
1A	01011000	6A	01010110	BA	01011101
1B	11011000	6B	11010110	BB	11011101
1C	00111000	6C	00110110	BC	00111101
1D	10111000	6D	10110110	BD	10111101
1E	01111000	6E	01110110	BE	01111101
1F	11111000	6F	11110110	BF	11111101

Table 3-5. Hex to Binary Conversion (Cont.).

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
20	00000100	70	00001110	C0	00000011
21	10000100	71	10001110	C1	10000011
22	01000100	72	01001110	C2	01000011
23	11000100	73	11001110	C3	11000011
24	00100100	74	00101110	C4	00100011
25	10100100	75	10101110	C5	10100011
26	01100100	76	01101110	C6	01100011
27	11100100	77	11101110	C7	11100011
28	00010100	78	00011110	C8	00010011
29	10010100	79	10011110	C9	10010011
2A	01010100	7A	01011110	CA	01010011
2B	11010100	7B	11011110	CB	11010011
2C	00110100	7C	00111110	CC	00110011
2D	10110100	7D	10111110	CD	10110011
2E	01110100	7E	01111110	CE	01110011
2F	11110100	7F	11111110	CF	11110011
30	00001100	80	00000001	D0	00001011
31	10001100	81	10000001	D1	10001011
32	01001100	82	01000001	D2	01001011
33	11001100	83	11000001	D3	11001011
34	00101100	84	00100001	D4	00101011
35	10101100	85	10100001	D5	10101011
36	01101100	86	01100001	D6	01101011
37	11101100	87	11100001	D7	11101011
38	00011100	88	00010001	D8	00011011
39	10011100	89	10010001	D9	10011011
3A	01011100	8A	01010001	DA	01011011
3B	11011100	8B	11010001	DB	11011011
3C	00111100	8C	00110001	DC	00111011
3D	10111100	8D	10110001	DD	10111011
3E	01111100	8E	01110001	DE	01111011
3F	11111100	8F	11110001	DF	11111011
40	00000010	90	00001001	E0	00000111
41	10000010	91	10001001	E1	10000111
42	01000010	92	01001001	E2	01000111
43	11000010	93	11001001	E3	11000111
44	00100010	94	00101001	E4	00100111
45	10100010	95	10101001	E5	10100111
46	01100010	96	01101001	E6	01100111
47	11100010	97	11101001	E7	11100111
48	00010010	98	00011001	E8	00010111
49	10010010	99	10011001	E9	10010111
4A	01010010	9A	01011001	EA	01010111
4B	11010010	9B	11011001	EB	11010111

Table 3-5. Hex to Binary Conversion (Cont.).

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
4C	00110010	9C	00111001	EC	00110111
4D	10110010	9D	10111001	ED	10110111
4E	01110010	9E	01111001	EE	01110111
4F	11110010	9F	11111001	EF	11110111
F0	00001111	F6	01101111	FB	11011111
F1	10001111	F7	11101111	FC	00111111
F2	01001111	F8	00011111	FD	10111111
F3	11001111	F9	10011111	FE	01111111
F4	00101111	FA	01011111	FF	11111111
F5	10101111				

3.4.11 BIG BERT Display

The BIG BERT DISPLAY located to the right of the MAIN BERT DISPLAY is provided as a convenience for the user. This menu allows the selection and display of any two of the error measurement parameters which are accumulated by the Model 5500. The BIG BERT menu is a split screen, large format display as shown in figure 3-20. The user may choose a parameter for display by using the UP/DOWN CURSOR keys to place the half intensity block in the top or bottom half of the display. Then, using the select keys, the user may scroll through any of the parameters being measured and display whichever one is desired.

> ***NOTE***
>
> This does not interfere with the test in progress.

The BIG BERT display permits viewing any two parameters from a distance and is helpful when the test technician has to be some distance from the test set.

3.4.12 Other Menus

The optional displays (G.821, High Speed Jitter, MSU Configuration, etc.) are discussed in the options section of this instruction book.

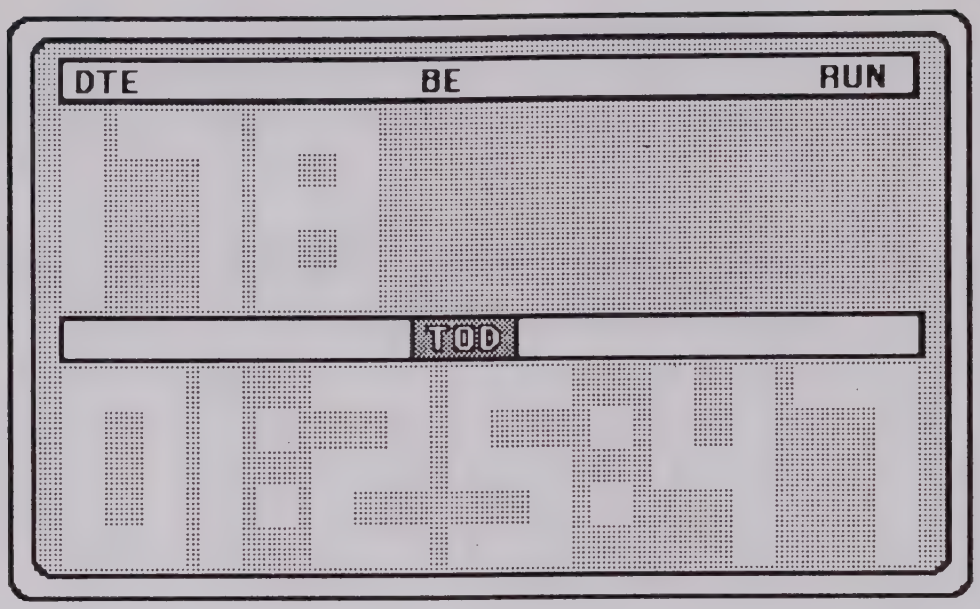
3.5 ACTIVITY INDICATORS

There are 12 green LED's on the 5500 front panel to indicate activity of the installed interface module.

The actual points being monitored are on the TTL interface between the module and control board. Since there are many different module options, all front panel indicators may not be applicable to a particular interface.

In addition, some of the indicators change meaning when modes are switched between DTE and DCE.

Tables 3-6 and 3-7relate the LED's to the interface circuit being monitored, for each module and mode of operation.



BIG BERT Display
Figure 3-20

The LED indicators provide interface activity status as well as mode (RUN), async, sync recovery and error injection status. These provide a quick visual indication of what is occurring at the interface and can often lead to rapidly identifying the source of a problem. For instance, if the Model 5500 is transmitting data and the TD LED is lit but there is no received data (RD LED not lit) then it is possible that the transmission source at the distant end is not functioning. This could be a modem which is receiving data but whose transmit section has become defective.

Table 3-6. RS-232/RS-449 Activity Indicators.

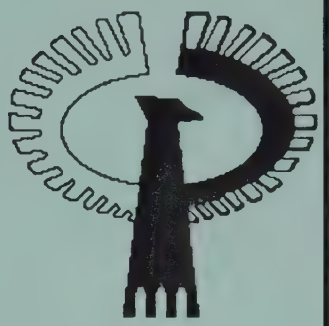
INDICATOR	ACTIVITY			
	RS-232		RS-449	
	DTE	DCE	DTE	DCE
TD/RD	Xmit Data	Rx Data	Send Data	Recount Data
RD/TD	Rx Data	Xmit Data	Receive Data	Send Data
RC/RC	Rx Clock	Rx Clock	Rec. Timing	Rec. Timing
TC/TC	Tx Clock	Tx Clock	Xmit Timing	Xmit Timing
RTS/DCD	Rqst to Send	5500 Data Carrier Det.	Rqst to Send	Rec. Ready
CTS/RTS	Clear to Send	Clear to Send	Clear to Send	Rqst to Send
DSR/DTR	DSR	DTR	Data Mode	Terminal Rdy
DTR/DSR	DTR	DSR	Terminal Rdy	Data Mode
DCD/CTS	Data Carrier Det.	Clear to Send	Receiver Rdy	Clear to Send
RI/RI	Ring Ind	Ring Ind	Incoming Call	Incoming Call
SQ/SQ	Signal Qual	Signal Qual	Signal Qual	Signal Qual
SCTE/SCTE	SCTE	SCTE	Terminal Tim	Terminal Tim

Table 3-7. T1/T1C and V.35 Activity Indicators.

INDICATOR	ACTIVITY			
			V.35	
	T1/T1C	FRAMED T1	DTE	DCE
TD/RD	Transmit Data	Transmit Data	Transmit Data	Receive Data
RD/TD	Receive Data	Receive Data	Receive Data	Transmit Data
RC/RC	Recovered Receive Clock	Gated Internal Clock	Element Timing Xmit Signal	Element Timing Xmit Signal
TC/TC	Recovered Xmit Clock	Gated Internal Clock	Element Timing	Element Timing Data Channel Rec
RTS/DCD	X *	X *	Request to Send	Line Signal Det
CTS/RTS	X	N/A	Ready for Sending	Request to Send
DSR/DTR	X	X	Data Set Ready	Data Terminal Ready
DTR/DSR	X *	X	Data Terminal Ready	Data Set Ready
DCD/CTS	X	X *	Receive Data Channel Receive Line Signal Detector	Drive Ready for Sending
RI/RI	X	X	Calling Indicator	Calling Indicator
SQ/SQ	X	X	X	X
SCTE/SCTE	Internal Clock Source	Gated Recovery Receive Clock	Transmitter Signal Element Timing (DTE Source)	Transmitter Signal Element Timing (DTE Source)

* May be control signals pertinent to internal 5500 functions on these monitored lines.

5500
Data Communications Analyzer



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4.1 GENERAL

Bit Error Rate Testing, whether at 75 bps rates or 1.544 Mbps rates, has a common purpose in digital circuit maintenance. That purpose is to determine whether or not a given transmission path can support a digital transmission without errors.

To test a digital circuit and determine whether or not errors are being generated it is customary to employ a test set which generates a known pattern and transmits it over the circuit. The circuit may be "looped" at the distant end or another test set may be located there. In any event, the pattern received is compared bit by bit to the known pattern generated and any discrepancies in the received pattern are counted as errors.

Since a known pattern must be substituted for the live traffic in order to perform a Bit Error test, these tests are often referred to as "out of service" tests.

The test patterns employed are pseudorandom or user sequences of binary digits which simulate live traffic. The term "pseudorandom" implies that the stream of bits only appears to be random. While the test pattern bit stream must appear to be random to simulate live traffic, it still must have some repetition in order for the test set to detect and recover the pattern.

Other patterns beside pseudorandom sequences are useful for test purposes, and not necessarily for Bit Error Testing. The Model 5500 provides a pattern generator capable of generating pseudorandom sequences of length 63 bits, 511 bits, 2047 bits, Reversed 2047 bits, (2^15)-1 bits, (2^20)-1 bits, and the Quasi-Random Word which is a (2^20)-1 bit long pattern with greater than 14 zero suppression. In addition, the Model 5500 pattern generator is capable of generating All Marks, All Spaces, Alternate Mark/Space, T1 CSU Set Code, T1 CSU Reset Code, FOX message, and USER input patterns of up to 135 characters in HEX.

The variety of digital equipments to be tested, both DCE and DTE, is so vast that the choice of pattern depends upon a number of factors. For example a pseudorandom sequence 63 bits long is fine for a low speed modem testing. At 300 baud or even 1200 baud the 63 pattern looks like regular traffic. However, if we attempted to use this pattern at higher data rates (T-1 for example) then the "random-like" nature of this pattern would disappear. It is also possible that certain pseudorandom sequences may generate long strings of zeros. Some systems have real problems with long strings of zeros. In particular, T-1 carrier systems operating at 1.544 Mbps, restrict data patterns to no more than 14 consecutive zeros.

As a rule of thumb, the choice of patterns follows the bit rate of the device or system under test. The higher the bit rate the longer the pattern and vice versa. Thus we see 511 patterns used for testing 1200 baud modems and the QRW used to test T-carrier systems.

No test set, no matter how good it is, can substitute for the experience of the operator when it comes to resolving a problem in the transmission path. All the test set can do is provide the tool for analyzing the symptoms of the problem and, if possible, increase the diagnostic ability of the technician by providing him with accurate information.

The Model 5500 increases the diagnostic ability of the user by measuring and displaying up to twenty-seven error parameters plus bias distortion, frequency, event, time, and optional jitter simultaneously. The Model 5500 places all of the analysis tools in one instrument and provides all of the test results simultaneously. This improves the user's ability to solve problems faster because the Model 5500 can simulate the problems (inject errors or jitter) and analyze the symptoms simultaneously to point the finger in the right direction as fast as possible.

To aid the user in making the most use of the Model 5500, the following section details and defines the various Bit Error Rate Testing parameters.

4.2 BERT DISPLAY OPTION DEFINITIONS

The definitions of the BERT parameters are provided to promote an understanding of what is being measured and how it is being measured.

ABE - ADJUSTED BIT ERRORS

Adjusted bit errors differ from the standard bit error function. Adjusted bit errors include, in addition to the standard in synchronization errors, an error count equal to one half the bait rate. For example, a unit may have the following totals:

Frequency = 1.544MHZ
BE = 12
SLS = Ø.25
ABE = 193Ø12
ETS = 1Ø
EFS = 9.45

The ABE parameter is calculated by taking the total BE (12), plus one half the bit rate (1.544EØ6/2), times the amount of time in sync loss (Ø.25), equals:

ABE = 12 + Ø.25 * (1.544EØ6/2) = 193,12

ABER - ADJUSTED BIT ERROR RATE

The adjusted bit error rate is calculated in a manner similar to bit error rate. The adjusted bit error rate is the number of adjusted bit errors divided by the total number of bits. From the example given in the ABE definition:

ABER = 193Ø12 / 1.544EØ6 = 12.5ØE-2

ALRM - ALARMS:

This parameter provides the user with information on the current, real time status of the receive side of the system under test and is available with the Model 5500-624 Framed T-1 Interface and 5500-628 ESF T1 Interface Options. Four or five alarm states are displayed in this block.

The alarm states for the 5500-624 module are as follows. The first alarm is B2. This

is the so-called YELLOW ALARM. It means that bit number 2, in each of the twenty four received PCM channels making up to the T-Carrier, was forced to zero for more than 50 milliseconds. This indicates that the terminal equipment at the remote end of the circuit has lost synchronization or that there has been no incoming DS-1 data for more than two seconds. The second state is indicated by an S. This character, when present on the display, indicates that signaling frame bit errors are occurring. The T-Carrier framing format is an interleaved pattern twelve bits in length. Six of these bits are signaling frame bits while the other six bits are terminal frame bits. The occurrence of 2 out 4, or 2 out of 5 frame bits in error will cause the terminal to try to resync. This can propagate a burst of errors down the line. The third state, loss of PCM, is indicated by a C on the ALRM display block. If a string of 14 or more consecutive zeros is received, or if no data transitions occur for 2 or more seconds, the C indication is displayed. The fourth state is indicated by an F on the ALRM display. This indicates that errors in the terminal framing bits are occurring. The presence of one or more of these four characters on the ALRM display indicates an abnormal condition which must be investigated and cleared before continuing with any error testing. The normal indication on the ALRM display is an all dots pattern (.....). The four states occupy the following positions (B2.S.C.F.), and any one or all could be present at one time. Note that these are qualitative and not quantitative indications. It is more important to know that these conditions exist than it is to count how often they occur. (refer to section 3 for ALRM display for 5500-628 module)

AHST - ALARM HISTORY

The alarm display above is a real time display and will indicate the presence of an alarm only when the alarm condition is present. The alarm history display is a record of any alarms that have occurred during the test period regardless of their current state. The alarm history format is the same as the alarm format.

BALS - BLUE ALARM SECONDS

A blue alarm (all ones) is a response by the DTE to the detection of a loss of signal. A blue alarm is also refered to as an Alarm Indication Signal (AIS). The 5500 detects blue alarms and reports them as blue alarm seconds. A blue alarm second is defined as a one second interval in which there was at least one blue alarm detected.

BE - Bit Errors:

The known generated pattern is compared, by the detector, to the received pattern on a bit by bit basis. Any received bit which does not agree with what is known to have been sent is counted as an error. The error data is accumulated in a 16 bit register which is accessed by the processor every 1 millisecond. No error occurrences can be left undetected to a probability of $1X10^{-16}$.

BER - Bit Error Rate:

The Model 5500 is capable of providing the user with two bit error rates. One is a continuous moving average bit error rate which changes as the number of bits received increases. This provides the user with a running indication of the "health" of the circuit under test at all times rather than forcing the user to set in a number of bits, wait for the unit to process the data, calculate a BER number for the test

length, and wait to be restarted to measure BER again. The user can, of course, force the Model 5500 to emulate other test sets by choosing a combination of block length and number of blocks in test to yield a specific bit length test. For example assume that the user desires to have the Model 5500 compute BER for a test length of 105 bits, Choose a block length of 103 bits/block and 100 blocks for the number of blocks to be tested and you have a total of 105 bits. Press RUN and at the end of the 105 bits the Model 5500 will stop. At that time the BER block will have a numerical result which is the BER for the 105 BITS. Of course the user could obtain 105 bits by using a 104 block size and 10 blocks to test or a 105 block size and 1 block to test.

The Bit Error Rate is calculated based upon the bit errors and number of bits received. The Model 5500 is capable of providing this calculation on an ongoing basis (running average) or a one time basis. The advantage of the running average bit error rate is that it allows the user to track the ups and downs as the test progresses rather than have to wait until the end of the test to get an answer.

$$BER = \frac{\text{Bit Errors}}{\text{Number of Bits Received}}$$

The BER is updated at least once per second while testing is underway since this is the minimum update rate of the CRT.

BITS - RECEIVED DATA BITS:

This parameter is presented in scientific notation as, for example, 3.9E06 which means 3.9 million bits have been received.

BLE - ERRORED BLOCKS:

This is the number of blocks received with at least one bit in error. A block error will be counted whether one error or fifty errors occurs during the block.

BLK - BLOCKS:

This is the number of blocks received by the Model 5500. This number steadily accumulates during a test and is composed of all blocks both errored and error free. Setting the block length on the Model 5500 (10^2 to 10^9) determines what the receiver looks for and calls a block. The Model 5500 will start to count blocks when it is running and has acquired sync.

CBE - CURRENT BIT ERROR

The current bit error parameter is the number of bit errors that have occurred over the immediate past five seconds. This gives the user a measure of recent bit errors to aid in determining if adjustments to the transmission facilities are having an immediate effect.

CBER - CURRENT BIT ERROR RATE

The current bit error rate is a measure of the bit error rate over the last five seconds. If a burst of errors occurs the current bit error rate should register the number of bit errors in the last five seconds divided by the number of bits in the last five seconds.

CRCE - CRC ERRORS

CRC-6 (cyclic redundancy check) errors can be detected on either in-service or out-of-service lines employing the extended superframe (ESF) mode of framing. CRC-6 uses a mathematical algorithm to check the contents of a superframe and results in a 6 bit code for the superframe. The CRC code of

each superframe is encoded as 6 bits in the following superframe. As each superframe is received and decoded, a CRC check is recalculated and compared to the CRC code that was sent over the span. If they do not match, then one or more errors occurred during transmission of the superframe.

As CRC-6 errors occur they are counted in a 16 bit binary counter. This counter is read every 20 milliseconds and the count is accumulated as a 48 bit binary number for reporting in the CRCE field of the 5500-628 Bert Menu.

CRER - CRC ERROR RATE

One more category pertaining to CRC-6 errors has been defined as CRCER/ES or CRC errors per CRC errored second. This parameter is nothing more than the number of CRC errors that occurred in the last CRC errored second. Its primary use is to print to an external printer the number of CRC errors that occurred within every CRC errored second. These numbers could then be tabulated to characterize the occurrences and frequency that CRC errors occurred.

CRES - CRC ERRORED SECONDS

A CRC errored second is defined as a one second window in which at least one CRC error occurred. CRC errored seconds in the 5500 are measured synchronously, which means a CRC error initiates the errored seconds timer. CRC errored seconds are available only during the ESF mode of operation.

CEFS - CRC ERROR FREE SECONDS

CRC error free seconds are defined in the 5500 as the number of seconds that have elapsed that contained no CRC-6 errors. The formula used for calculating CRC error free seconds by the 5500 is:

CEFS=ETS-CRES

Where ETS is the total number of elapsed test seconds and CRES is errored seconds as described above.

CSLP - CLOCK SLIP

See loop timing.

ED - ERRORED DAYS:

The number of days during which at least one bit error occurred. Useful in very long term testing or when testing in accordance with certain European specifications such as CCITT G.821.

EFB - ERROR FREE BLOCKS:

This is the number of blocks received without an error in them and is calculated as:

BLOCKS - ERRORED BLOCKS = ERRORED FREE BLOCKS.

EFS - ERROR FREE SECONDS:

This important parameter is often used to characterize a data link. It is defined as the number of seconds during which no errors have occurred. It is counted by the Model 5500 when the unit is running and has acquired sync. The total of ES plus EFS is equal to the ETS.

EFS% - PERCENT OF ERROR FREE SECONDS

The percent of error free seconds is a ratio of error free seconds to total elapsed seconds. It is computed as:

%EFS = [EFS/ETS] * 100

%1sD - PERCENT ONE'S DENSITY

The percent one's density is provided for T1/T1C modules and is a ratio of the number of one's bits to the total number of bits. It is displayed as a percentage and will display in inverse video if the density drops below 12.5%. An alternate pattern should yield about a 50% one's density.

ES - ERRORED SECONDS:

This parameter is one of the more important measurement results. An error second is said to have occurred if at least one error occurs in the one second interval. The Model 5500 measures "synchronous" errored seconds (a bit error event initiates the errored second timer). Errored seconds, like all measurements, will start to be accumulated by the Model 5500 when it has begun to RUN and it has acquired sync.

ESR - ERRORED SECONDS RATE:

This is the number of errored seconds divided by the number of seconds and is a moving average.

ESR = ES/ETS = ES/(ES+EFS)

This parameter can easily yield other qualitative results for the user. In particular, the user can derive the % of Errored Seconds and % of Error Free Seconds quite easily from ESR. To obtain the percent errored seconds simply multiply the numerical result in the ESR display window by 100. For example, assume the reading for ESR is 3.1 E-2. Multiplying 3.1 x 102 by 100 yields the result 3.1% Errored Seconds. The percent error free seconds can be easily calculated by subtracting the 3.1% from 100% which yields 96.9% error free seconds.

ET - ELAPSED TIME:

This is the elapsed test time in hours/minutes/seconds since the RUN/STOP switch was set to RUN and the Model 5500 acquired sync. Elapsed time will not accumulate if the unit is not in sync or during sync losses.

ETS - ELAPSED TIME IN SECONDS:

This is the elapsed test time given in total seconds as opposed to the hours/minutes/seconds given by ET.

FBE - FRAME BIT ERRORS

Frame bit errors are detected by the 5500 by comparing the input data stream to the known FT frame bit sequence. The frame bit sequence is a result of adding one frame bit every 192 information bits. Violations of the frame bit sequence within the superframe are declared as frame bit errors and are counted in a 16 bit binary counter. This counter is read every 20 milliseconds and the count is accumulated as a 48 bit binary number for reporting in the FBE field of the 5500-628 Bert Menu.

FBER - FRAME BIT ERROR RATE

The frame bit error rate is defined as the rate at which FT framing errors are being detected. Unlike bit error rates which can only be determined on known bit patterns, the 5500 can provide the user with a continuous frame bit error rate, regardless of the data but only for framed data, which changes as the number of frame bits re-

ceived changes. This continually changing rate provides the user with a constant indication of the "health" of the line under test.

The frame bit error rate is calculated by the 5500 using the following formula:

FBER=Frame bit errors/Total
FT bits received

FBES - FRAME BIT ERRORED SECONDS

A frame bit errored second is defined as a one second window in which at least one FT frame bit error occurred. Frame bit errored seconds in the 5500 are measured synchronously (a framing error initiates the errored seconds timer). Frame bit errored seconds are available during all framed modes of operation.

FEFS - FRAME BIT ERROR FREE SECONDS

Frame bit error free seconds is another measure of the performance level of a circuit using some form of framing, either D4 or ESF. It is defined as the difference of total elapsed test seconds minus the frame bit errored seconds that occurred over the total test seconds and is calculated by the 5500 using the formula FEFS=ETS-FBES.

In this case, ETS is the total number of seconds of testing regardless of pattern sync.

FLOS - FRAME SYNC LOSS

A signal is in frame sync if not more than 2 out of 5 Ft bits are in error. It is out of sync if 2 or more out of 5 Ft bits are in error.

When frame sync is lost, the loss is counted by a 16 bit counter which is read every 20 milliseconds and accumulated in a 48 bit register for long term storage. Since the software can only get around to check the frame sync status every 20 milliseconds, it assumes that all sync losses that may have actually been of a much shorter duration, to be a loss of 20 milliseconds. The parameter displayed for the user pertaining to frame sync is Frame Sync Losses (FLOS) and is incremented every time frame sync is lost.

FLS - FRAME LOSS SECONDS

The frame loss seconds parameter is provided for T1/T1C modules. It is a measure of the number of seconds the data has been unframed. Frame loss seconds measures down to Ø.Ø1 seconds and displays three significant digits. Therefore, 1Ø.14 would be displayed as 1Ø.1 seconds.

LOOP TIMING

Loop timing was implemented in the 5500-628 interface module in order to tell the user whether the circuit under test is loop timed. All timing information is transmitted isochronously as part of the 1.544 Mb/s bipolar signal. Isochronous timing indicates that a clock is extracted from the incoming signal and is used to provide timing to the outgoing signal. A loop timed circuit is defined as frequency locking the oscillators which clock the outgoing 1.544 Mb/s signal to the long term average frequency of the incoming 1.544 Mb/s signal. An advantage of a loop timed circuit is the reduction of frame slips incurred when a receiving device receives a signal of one frequency and then re-transmits at a slightly different frequency.

The received signal has its clock extracted from the signal as a normal mode of operation. The signal present at the transmit side of the 5500 also has its clock extracted from it. These two clocks are then each fed into a 16 bit free running counter. Upon power-up

16 bit free running counter. Upon power-up and immediately after a clear sequence, the software latches both counters simultaneously and reads the current counter values. From these two values an initial delta (DELTAI) is computed which becomes a reference point. DeltaI is also stored as DELTA1 from which comparisons are made. From then on, until another clear is encountered, the two counters are read every 20 milliseconds and additional delta (DELTA2) is computed.

The two deltas (DELTA1 and DELTA2) are then compared. If they are the same or have not deviated by more than 40 clock counts, the circuit is assumed to be loop timed. If they are different by more than 40 counts the circuit is not loop timed.

The SLIP RATE parameter is simply the rate at which the two clocks are changing. The 5500 divides the current clock count by the total elapsed test seconds to derive the slip rate. The units for slip rate are thus counts per second.

Two other parameters are defined as WANDER+ and WANDER-. These parameters are the maximum positive clock count and the maximum negative clock count, respectively. If a circuit is loop timed but has some amount of wander (defined as jitter less than 10 Hz), these two parameters will show that amount deviating about the reference point. If a circuit is definitely not loop timed, then one or the other wander parameters will be constantly changing at the same rate and direction.

LOS - LOSS OF SYNC:

This parameter is based upon a bit error rate threshold being crossed. That is, when the bit error rate becomes excessively high, the Model 5500 will at some point, declare that it has lost sync and will not recover sync until the bit error rate drops below the threshold. The sync loss threshold in the Model 5500 is adjustable. It is factory set for initiating a sync loss whenever any 1000 bits received contains 100 or more errors. That is a BER 10-1 or higher. When the Model 5500 is out of sync, error parameter collection is meaningless and therefore only the time the unit is out of sync is accumulated.

MDY - MONTH/DAY/YEAR:

The month, day, year are available to date stamp any events printed out. The setting is retained in non-volatile memory. The settings are changed like any other parameters from the BERT FORMAT menu. These settings should be reviewed to account for leap year or other factors affecting the read out.

PF - POWER FAILURES:

The Model 5500 will count power failures to its input power supply. The threshold for counting a power failure is 90 Volts AC (180) Volts AC if operating from 1 220-240 VAC source). or less. The enables the operator to determine whether or not AC power was continuously available during long term unattended tests. Note that upon powering up the Model 5500, a power failure will be indicated so the user should always press the CLEAR "soft key" at the lower right of the main BERT CRT display before doing any testing.

RBPV - RECEIVE BIPOLAR VIOLATIONS:

These are bipolar violations of the AMI line code which occur on the receive pair. Unlike the TBPV parameter, BPV's on the

when the Model 5500 is operating in the TERMINATED mode as well as the BRIDGE mode.

RVFS - RECEIVE VIOLATION FREE SECONDS:

The count of the number of seconds on which no violations occurred on the receive pair of the T-Carrier under test.

RVR - RECEIVE VIOLATION RATE:

The rate at which receive BPV's occur. The RVR parameter can be measured in both the BRIDGED and TERMINATED modes. It is calculated as:

$$RVR = \frac{\text{RBPV (violation/bit)}}{\text{number of bits}}$$

RVS - RECEIVE VIOLATION SECONDS:

This is a count of each second in which at least one receive violation occurs.

SLS - SYNC LOSS SECONDS:

This represents the total accumulated time the unit is out of sync. A single sync loss of very short duration (much less than 1 second) will not cause the SLS counter to record. The sync loss itself will be counted but a sync loss second is not necessarily counted. The counter will, however, accumulate the outage time so that, for example, if each sync loss had a duration of 200 milliseconds then after 5 such occurrences the counter would increment and display a 1 in the SLS block. It is important to note that the information is not lost but only waiting for the total outage to reach 1 second.

TBPV - TRANSIT BIPOLAR VIOLATIONS:

This parameter is the count of violations of the Alternate Mark Inversion (AMI) bipolar line code format used for T1 and T1C transmission in the U.S. In this case, the BPV's are being monitored on the transmit pair of four wire T-Carrier system, hence the designation TBPV. This parameter is only measured by the Model 5500-600 module option operating in the Bridge Mode. In this mode this interface option has two receivers active and can monitor both the transmit pair and the receive pair of a full duplex T-Carrier. Transmit line bipolar violations, TBPV, may be measured in the BRIDGE mode, or may be injected at a programmed rate (but not measured) in the TERMINATE mode when the Model 5500 transmitter is enabled.

TOD - TIME OF DAY:

The time of day in hours, minutes, and second is available to time stamp any events printed out. The setting is retained in nonvolatile memory.

TVFS - TRANSMIT VIOLATION FREE SECONDS:

The number of seconds without a bipolar violation. The sum of TVS and TVFS equals the elapsed time in seconds (ETS).

TVR - TRANSMIT VIOLATION RATE:

The rate at which transmit BPV's occur. The TVR parameter can be measured only in the BRIDGED mode. It is calculated as:

$$TVR = \frac{\text{TBPV}}{\text{number of bits}} \text{ (violations/second)}$$

TVS - TRANSMIT VIOLATION SECONDS:

This is a count of each second in which at least one bipolar violation occurs. It is similar in usage to errored seconds (ES).

WND+ - WANDER POSITIVE

See loop timing.

WND- - WANDER NEGATIVE

See loop timing.

YALS - YELLOW ALARM SECONDS

A yellow alarm is the result of a customer's terminal equipment not being able to synchronize on the DS1 signal from the network. In response to this failure, the terminal equipment must issue a yellow alarm. Also, equipment recognizing a red alarm (out of frame condition for 2.5 seconds or more) should transmit a yellow alarm in the opposite direction.

A yellow alarm is indicated in D4 framing mode by setting bit 2 of 255 consecutive channels to a zero. In the ESF mode, a yellow alarm is indicated by 16+/-1 sets of alternating eight 1's /eight 0's pattern in the 4 Kb/s data link.

The 5500 detects yellow alarms in both modes of framing and reports them as yellow alarm seconds (YALS). A yellow alarm second is defined as a one second interval in which there was at least one yellow alarm detected.

15Z - 15 ZEROS

15 zeros is a measure of the number of times the T1 bit stream has contained 16 or more consecutive zeros.

15ZS - 15 ZERO SECONDS

15 zeros seconds is the count of the number of seconds that have had one or more 15 zeros condition.

4.3 BER TEST ASSISTANCE

Table 4-1 presents a list of possible problem areas if the Model 5500 does not achieve synchronization with the device under test.

4.4 USER PATTERN GENERATION

The user pattern allows the user to construct a pattern for transmission by the Model 5500. Selecting the USER pattern causes the Model 5500 to transmit a repetitive pattern of whatever the operator has placed in the USER PATTERN display. The user is permitted to enter up to 135 characters in HEX from the front panel HEX keypad or from a printer over the Remote Control ports. Each character in HEX is an 8 bit long word so the total bit length which could be input is 1080 bits. However, the user may enter as few as three characters if desired.

> ***NOTE***
>
> With no characters installed it is possible that the Model 5500 will, power up, default to the system menu and flash the USER PATTERN memory block. This "error" can be ignored or the user may choose to place three or four characters into the User Pattern display. These can be any HEX characters the user may want to place in memory. Refer to section 3.4.11 of this instruction book for more detail on USER PATTERN function.

4.5 GRAPH DISPLAY

The GRAPH DISPLAY located at the left of the MAIN BERT DISPLAY in the menu matrix provides the user with an important tool in locating the source of a problem.

Often, the cause of a burst of errors may be related to its time occurrence. That is, a large air conditioner or other high power device may cycle on and the surge may cause a nearby terminal or modem to suffer a power line hit. The events can be correlated to the cause using the GRAPH DISPLAY.

The operator may choose to plot up to four different error parameters versus time so as to generate a more complete picture of circuit conditions.

A typical graph display of bit errors is shown in figure 3-16. A typical test set up might involve graphing bit errors, sync losses, bipolar violations (T-Carrier testing), and errored blocks. Other parameters can be graphed but generally speaking, the above are the most important in isolating problems. The set up of the GRAPH display is described in detail in section 3.4.8.

Table 4-1. BER Test Assistance .

PROBLEM	CORRECTIVE ACTION
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Check bit rates, sync/async mode, character size, parity etc. Verify that correct mode (DCE or DTE) has been selected. Verify that correct mode (RTS/DCD) has been selected. Verify that BRIDGE mode in T-Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwiseproperly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units. Also, in SYNC mode, ensure that one unit supplies clock and the other is set to EXT clock.

Table 4-1. BER Test Assistance (Cont.).

PROBLEM	CORRECTIVE ACTION
SYNC LED blinks on and off in synchronous testing	If two test sets are operating in an end to end test verify that one is set to supply clock (internal timing) and the other is set to EXTERNAL clock. If a modem or other device in the circuit is the master clock, set both sets to external. Note: There can be only one Master Clock in a synchronous circuit.
SYNC LED not illuminated and TD LED is off	Verify that RTS is activated if unit is configured as DTE.
Constant bursts of errors detected in testing synchronous devices	Select External clock mode if not already selected. (Most synchronous devices are strapped to supply clock).
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when set stops. This is normal operation.
Model 5500 displays errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. Note that T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.
RAM error on power-up	Battery may be discharged. Leave power on unit for 24 hours to charge up battery.

The graph display stores up to sixty hours of data in up to one minute intervals if only one parameter is graphed. This permits long term unattended testing (over a weekend for example) without losing the data, or when it occurred.

When setting up a GRAPH DISPLAY for a long term test it is suggested to set the HORIZONTAL time scale to sixty minutes per division and the VERTICAL scale to x1 for the maximum sensitivity. This will cause even single events to be displayed. When the user wishes to view the display the scales can always be changed for a more convenient display. No data is lost by changing the scales.

The user also can print out the graphic data (for a single parameter). The Model 5500 will print out data continuously in 1, 10, or 60 minute increments depending upon the horizontal scale setting and the user can therefore bypass the 60 hour limitation of the GRAPH DISPLAY itself.

Figures 3-14 and 15 detail the setup for graph data (GRAPH DATA SELECTION). Figure 3-16 details the actual graph display and display controls. Table 4-2 presents the graph definitions. The Model 5500 graph is provided only under local control. For remote control operation, an intelligent controller may by utilized to obtain data plots.

4.6 FREQUENCY MEASUREMENT

The Model 5500 is also a frequency counter with a resolution of 0.1 HZ below 1 MHZ and 1 HZ above 1 MHZ. The reading is displayed on the main BERT menu as shown in figure 3-9. The user may select BR to view the Asynchronous Baud Rate, or TC (Transmit Clock), RC (Receive Clock) or XC (External Clock) in synchronous system testing.

The Model 5500 counter provides the user with a reasonably accurate diagnostic tool for uncovering frequency related error problems. This enables the user to spot a drifting clock. When the test set is set up in the EXT Clock mode, the user can measure and determine the stability of the Receive Clock by selecting RC. When acting as a synchronous DTE it is convenient to check the outgoing clock by selecting TC. The user can easily compare the Transmit and Receive clocks for significant differences. When a USER clock input to the rear panel BNC connector has been selected the user can measure it on the TC of Transmit Clock field.

The user may measure the external clock (Pin 24 on the RS-232 interface module) signal by selecting XC. This would be used when the Model 5500 is deriving its clock from an external source such as a modem or terminal to time its transmitter.

Frequency counter display accuracy is a function of the stability of the internal 4.608 MHZ reference clock oscillator. The Model 5500 uses a software controlled correction to zero out the impact of the crystals in accuracy and so all that remains is the effect of thermal stability or drift. This is typically less than 5 parts per million with the standard crystal and can be reduced to 1 part per million or less with the precision clock (Model 5500-CL01) option.

The software controlled calibration command for the frequency counter - TWEAK - is described in detail in section 4.9, REMOTE PROGRAMMING, Table 4-3 and the procedure for the TWEAK adjustment is found in section 5, the maintenance section, of this instruction book.

Table 4-2. Graph Definitions.

SYMBOL	DEFINITION
Crsr 1	The main cursor for the graph used to determine the exact time and magnitude of the data being plotted. The **UP SELECT** key advances the cursor in the time increments set by the horizontal resolution. The **DOWN SELECT** key backs up the cursor in time. A time of day clock reading is provided next to the Crsr 1 display.
Crsr 2	Cursor 2 is used for the plot printing function. Data between Cursor 1 and Cursor 2 can be printed out by depressing the SOFTKEY corresponding to 1-2 in the PRINT SELECTION menu.
Horizontal (Horiz)	CRT field that displays the time scale selected. One, ten or sixty minutes per division may be selected. Thirty time divisions can be displayed without scrolling to the right. The resolution decreases as the number of parameters to be graphed increases.
Vertical (Vert)	CRT field that displays the vertical scale factor. Factors from 1 to 100,000 are provided.
Mag 1	Displays the magnitude of the data at Cursor 1 position.
Mag 2	Displays the magnitude of the data at Cursor 2 position.
ALL	Softkey used to print entire sixty hour graph plot. Will also enable continuous printout of graph data.
1-2	Prints graph data between Cursor1 and 2 only.
DAT	Softkey used to select numerical data print out instead of graphic data. Used with any standard RS-232 interface printer.
GRAPH DATA	CRT field used to select data parameter(s) to be plotted.

4.7 EVENT TIMING

The Model 5500 measures the time interval between transitions of any two selected interface signals to 4.67 minutes duration with a resolution of 1 microsecond to 10 milliseconds depending upon scale.

RTS /	DTR /
RTS \	DTR \
RD /	DCD /
RD \	DCD \
TD /	DSR /
TD \	DSR \
SQ /	CTS \
SQ /	CTS \

The "/" character after a signal indicates that signal going "TRUE". For an RS-232 interface, a MARK to SPACE (1 to 0) Transition is the TRUE condition. The "\" character shows a transition to FALSE. On a TTL interface a "HIGH" to "LOW" transition is the TRUE condition. If an "I" is displayed, valid transitions have occurred, and an "I" for Indeterminate is shown.

The user selects the resolution as 1US, 10US, 100US, 1MS, or 10MS, and then chooses which two events are to be measured. The Model 5500 automatically measures the time delay between the transitions, and updates the measurements display on a continuous basis.

4.8 BIAS DISTORTION (SKEW)

The Model 5500 measures BIAS DISTORTION on the receive data lines. A pattern having a uniform 50/50 distribution of 1's and 0's is customarily used as the transmitted signal. Any of the Model 5500 pseudorandom sequences may be used.

Bias is determined as a ratio of MARKS (1's) to SPACES (0's) and expressed as a percentage.

A reading of 0% indicates a constant SPACE signal while a reading of 100% indicates a constant MARK signal. A 50% reading indicates ideal symmetry of MARK bit widths periods to SPACE bit widths periods.

A reading of 45% to 55% is considered acceptable in most systems. Some older modems may have larger windows of acceptable performance but in general readings outside the 45-55% range maybe cause for further investigation.

If a modem or other device has filters shaping the bit stream, and they have degraded band pass characteristics which favor 1's over 0's or vice versa then the likelihood of an error occurring is increased.

Bias Distortion was more of a problem with older FSK type modems employing lumped element filters than it is with modern modems which use digital filter techniques.

Bias Distortion measurement accuracy is +1%, and the reading is updated at least once per second.

4.9 REMOTE CONTROL

The Model 5500 remote control ports permit the user to control the 5500 from a computer or dumb terminal. Both IEEE-488 and RS-232 ports are provided. Both connectors are located on the rear panel of the 5500. Before connecting the 5500 to one of the remote ports, the remote port must be selected and the remote port characteristics must be configured to match the computer or terminal characteristics.

4.9.1 Initial Setup

Select the Remote Configuration menu on the Model 5500 (refer to figure 4-2). This menu is used to set the 5500 characteristics to match those of the terminal or computer to be used as the remote control device. Enabling the TRACE on the menu will permit the user to view the character streams being sent between the 5500 and the terminal. Data from the terminal will appear on the left of the screen on the second line from the top (the line with the] [in the center) while the data from the 5500 to the terminal will appear on the same line to the left.

The Model 5500 operates using the 7 bit ASCII code. Commands to the 5500 consist of strings of ASCII characters in the range from space (20_H) to DEL ($7F_H$) terminated by a carriage return ($ØD_H$).

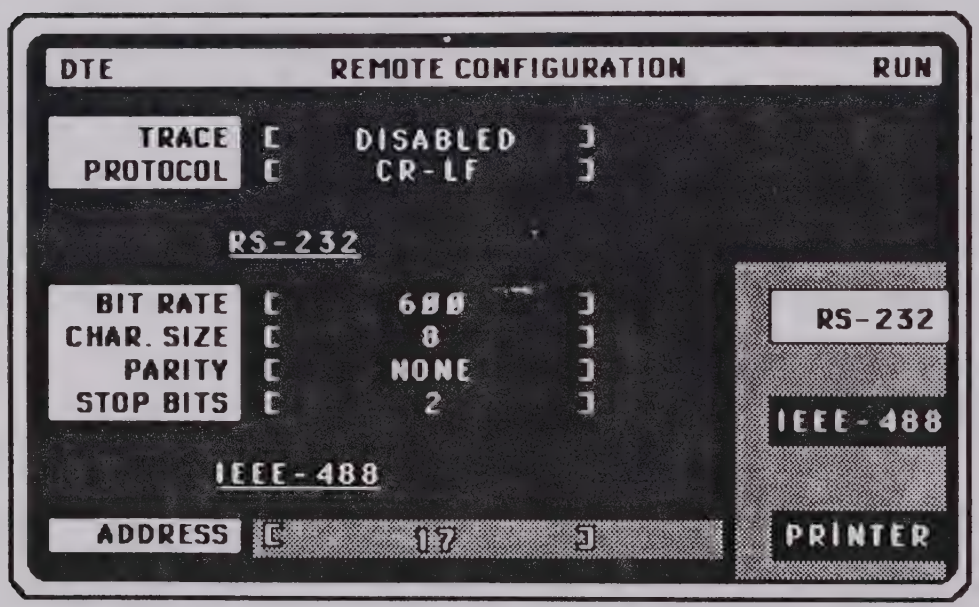
The response from the Model 5500 can take on one of several formats depending upon the selected protocol.

a) IEEE-488/CRLF

In this mode, commands which result in the Model 5500 sending a response, expect it to be formatted as follows:

Char
"
"
Char x
CR
LF EOI

The controlling device should be set to terminate its input on either the line feed character code or the assertion of the EOI line.



Model 5500 Remote Configuration Menu
Figure 4-1

b) IEEE-488/ACK

Unlike the previous mode, in which the controller operated in an open loop manner, the ACK protocol provides a response to each command regardless of whether the command returns data. If the command is understoood an ACK (06_H) character is returned. If an error is encountered in interpreting the command, NAK (15_H) is returned. If additional data is to be returned it follows the first ACK and is terminated by a second ACK. three possible responses are shown below:

(error)	NAK EOI
(good, no data)	ACK EOI
(good, data)	ACK Char 1 " " Char x ACK EOI

In all cases the EOI line indicates end of response.

c) RS232/ACK

Operation of the RS-232/ACK protocol is identical to the IEEE-488 protocol with the exception that there is no EOI line. It is the controllers responsibility to know whether or not additional data is expected following the first ACK. In practice this knowledge comes naturally with the program organization.

This protocol uses a half duplex data transfer structure on the RS232 port. The Model 5500 controls data flow to itself through the DTR line and sends data via the RTS/CTS handshake.

d) RS232/CRLF

This mode is intended primarily for use with a directly connected terminal. It operates full duplex and echos every character received. In this mode, DEL and <Back Space> send a character sequence, the response to which will delete the last character. A <Control X> will cause the Model 5500 to ignore the present line. If an error is encountered in interpreting the input line, it is reprinted to the error point and a question mark (?) is inserted. The response to the command is shown on the line following the command.

When a protocol has been selected, use the cursor movement, cursor select keys, and softkeys to make the Remote Port Configuration menu, as shown in figure 4-1, match the selected characteristics. In the example shown in figure 4-1, RS232 has been selected by pressing the top softkey. Then by using the cursor movement and cursor select keys, the TRACE mode was enabled, CR-LF protocol was selected, the Bit (Baud) Rate was set to 1200 bps, the character size was set to 8, parity was set to none, and the number of stop bits was set to one.

4.9.2 Electrical Connection

4.9.2.1 RS232 Port

The Model 5500 is shipped from the factory with its RS-232 port configured as a DCE. That is, it is emulating a modem expecting a printer or terminal to be connected to it. If it is desired to connect a modem to the port, a null modem cable must be used, or the internal dip switches within the 5500 must be changed to the DTE position. Refer to section 2 of this manual for instructions regarding this change. The RS-232 port pin assignments are as follows:

PIN	FUNCTION	SOURCE
3	RD	USER
2	TD	5500
5	CTS	USER
4	RTS	5500
20	DTR	5500
8	DCD	USER

4.9.2.2 IEEE-488 Port

The IEEE-488 Bus enables the simultaneous connection of up to 31 instruments to a single controller. The system operates by prefacing each data packet with an address. It is thus necessary for the user to select a numeric address (0-30) for the Model 5500. Then it will 'listen' on the bus and respond to any commands prefaced by its address. The IEEE-488 port pin assignments are shown below:

PIN	FUNCTION	PIN	FUNCTION
1	D101	2	D102
3	D103	4	D104
5	E10	6	DAV
7	RFD	8	DAC
9	IFC	10	SRQ
11	ATN	12	CHASSIS
13	DIOS	14	D106
15	D107	16	D108
17	REN	18	GND
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND

4.9.3 Command Description

Commands to the Model 5500 are divided into two basic types. The first command type, configuration commands, is used to configure the test setup. Commands of the second type, result commands, are used to read the test results.

Configuration commands have three formats. The first format is the command issued by itself (for example **BR** for bit rate). When issued with no parameters, all of the configuration commands return their present setting. The second format is to follow the command with a question mark (?) in the parameter field (for example **BR ?**). In response to this format, the 5500 returns either a list of all possible settings for this command or a description of the parameter setting format. The third format is the command followed by a valid parameter. This results in the immediate update of the selected function to the specified state (for example **BR 9600** sets the bit rate to 9600 bps).

The second command type, the results commands, is used to read test results. These commands ignore any data past the command field and always return the present value of the selected function. In most cases, the value returned in response to one of these commands is a snap-shot of the parameters value at the instant the command is evalutated. The exceptions to this are event time, frequency measurement, and bias. These three measurements are configured such that repeated requests will result in a newly measured value for each response. This allows for the gathering of meaningful data in cases where statistical analysis will be done on the readings.

> ***NOTE***
>
> This can result in response delays of up to 10 seconds when reading event times and approximately one second when reading either frequency or bias.

In addition to the command types described above, certain commands are dependent upon the type of interface. At the present, these are divided into commands which function with all interface modules, those which function only with the T1/T1C interface, and those which function with any interface other than T1/T1C. In the following tables which define all the commands, this is noted with an ALL for all, T1/T1C for T1/T1C only, OTHER for other than T1/T1C and specific module name where command is only applicable to a single module.

The question mark (?) is a special command. Entering the question mark following the prompt (B>) will return the Help menus as shown in figure 4-2. These menus list all the system command words and a brief command description.

```
B>?
      HELP MENU --- "A" or "a" aborts

SYSTEM:                      ESTART...Event Start        ESTOP....Event Stop
?.........This Help Menu                                 EVENT....Event Time
DISPLAY..Display Menu        LPMODE...Loop Mode B-303
DSPCRT...CRT Disp on/off     PROTECT..Parameter Prot.    SIM......DTE/DCE Select
DTR/DSR..Control State       RING.....Ring Mode B-303    STATUS...System Status
INTERFACE.I/F Type           RLOCK....MSU Rem. Lockout   SYNC.....SYNC State
INVERT...Invert Td Rd etc.   RTS/DCD..Control State      TOD......Time of Day
LOCK.....Parameter Lock      RX0-3....Spare Receivers    TWEAK....Freq. Cal.
LOOP.....Tx to Rx Loop       SCRNSAV..Scrn Savr on/off   TX0-5....Spare Drivers
                             SIGQ.....SIG QUAL B-303     UNLOCK...Param. Unlock
PRINTER:                                                 VER......Version No.
GRAPH....Graph Setup
PEND.....ACK/NAK Poll        PRINT....Print Setup
                             ^C.......Cancel Print
EVENT TIMING:
ESCALE...Timer Scale


<more>
```

Model 5500 Main Help Menu - Screen 1
Figure 4-2

```
USER PROGRAMS, PATTERNS AND SEQUENCES:
                     STORE....User Prog
                     USRPAT...User Pat. Edit


                     JAVG(H)..Average Jitter
                     JPP(H)...P-P Jitter


                     HJFREQ...Cursor Frequency
                     HJGENAMP.Gen. Amplitude
                     HJLINE...Albo Value
```

Model 5500 Main Help Menu - Screen 2
Figure 4-2

```
      BERT:
ABE......Adj. Bit Errors     DMODE....DDS Test Mode       PlsD.....Percent 1s Den.
ABER.....ABE Rate            DRIVE....DDS Drive Polar.    PAT......Pattern
AHST.....Alarm History       EBR......Erred Blk Rate      PR.......Parity
ALARM....Alarms              ED.......Elapsed Days        R/S......R/S State
AUTOSYNC.Auto Sync Break     EFB......Err Free Blocks     RBPV.....Receiver BPV
BA.......Blks Analyzed       EFS%.....Percent EFS         REXMIT...Rexmit Mode
BE.......Bit Errors          EFS......Err Free Seconds    RUN......Start Test
BER......Bit Error Rate      ES.......Errored Seconds     RVFS.....Rx BPV Free Sec
BIAS.....Bias                ESR......Erred Sec Rate      RVR......Rx BPV Rate
BITS.....Bit Count           ET.......Elapsed Time        RVS......Rx BPV Seconds
BLE......Block Errors        ETS......ET Seconds          SB.......Stop Bits
BLKS.....Num. of Blocks      FLS......Frame Loss Secs     SIMPLEX..DDS Simplex Loop
BPVRATE..BPV Inj. Rate       FRAME....Frame Enb/Dis       SLS......Sync Loss Seconds
BR.......Bit Rate            FSRC.....Meas. Freq. Src.    STOP.....Stop Test
BS.......Block Size          INJ......Error Inject        TBPV.....Xmtr BPVs
CBE......Curr. Bit Errors    INJMODE..Inject Mode         TDCLK....DCE SYNC Tx Clock
CBER.....CBE Rate            IRATE....BE Inject Rate      TVFS.....Xmtr BPV Free Sec
CLR......Clear               LOSS.....# of SYNC Losses    TVR......Xmtr BPV Rate
CODE.....Line Code           MD.......Mode                TVS......Xmtr BPV Seconds
CS.......Character Size                                   TXAUTO...Tx Auto Resync
```

Model 5500 Main Help Menu - Screen 3
Figure 4-2

```
BER......Bit Error Rate      ES.......Errored Seconds     RVFS.....Rx BPV Free Sec
BIAS.....Bias                ESR......Erred Sec Rate      RVR......Rx BPV Rate
BITS.....Bit Count           ET.......Elapsed Time        RVS......Rx BPV Seconds
BLE......Block Errors        ETS......ET Seconds          SB.......Stop Bits
BLKS.....Num. of Blocks      FLS......Frame Loss Secs     SIMPLEX..DDS Simplex Loop
BPVRATE..BPV Inj. Rate       FRAME....Frame Enb/Dis       SLS......Sync Loss Seconds
BR.......Bit Rate            FSRC.....Meas. Freq. Src.    STOP.....Stop Test
BS.......Block Size          INJ......Error Inject        TBPV.....Xmtr BPVs
CBE......Curr. Bit Errors    INJMODE..Inject Mode         TDCLK....DCE SYNC Tx Clock
CBER.....CBE Rate            IRATE....BE Inject Rate      TVFS.....Xmtr BPV Free Sec
CLR......Clear               LOSS.....# of SYNC Losses    TVR......Xmtr BPV Rate
CODE.....Line Code           MD.......Mode                TVS......Xmtr BPV Seconds
CS.......Character Size      MFREQ....Meas. Freq.         TXAUTO...Tx Aauto Resync


      G703 OPTION:
G7BYTE...g703 Byte Sync      G7ROT....g703 R.Oct.Tim      G7SRT....G7SRT Rate
G7CSRC...g703 Clk.Src.       G7SAMP...g703 Sampl.Edge     G7TLV....g703 Tx Level
G7MODE...g703 Mode           G7SELM...g703 Sel.Meas.      G7TOT....g703 T.Oct.Tim
G7OCTT...g703 Oct.Tim.       G7SELV...g703 Sel.Var.

B>
```

Model 5500 Main Help Menu - Screen 4
Figure 4-2

4.9.3.1 System Commands

The system commands are configuration commands. They are listed in table 4-3.

Table 4-3. Model 5500 Remote System Commands.

COMMAND	FUNCTION	INTERFACE
?	Returns screens as shown in figure 4-2.	ALL
DISPLAY	Returns menu displayed on 5500	ALL
DISPLAY ?	Returns BERT, FORMAT, PROG, PAT, PRINT, CONFIG, GRAPH, REMOTE BLACK, BIG, JITTER, MSU, G821 G-SELECT	ALL
DISPLAY xx	Changes menu displayed on 5500 to menu selected from list above	ALL
DSPCRT	Returns status of the 5500 CRT display	ALL
DSPCRT ?	Returns "ON, OFF"	ALL
DSPCRT xx	Sets 5500 CRT display on or off	ALL
DTR/DSR	Returns state of DTR/DSR line	Other
DTR/DSR ?	Returns "Enter "T" for TRUE or "F" for FALSE"	Other
DTR/DSR xx	Sets state of DTR/DSR line to true or false	Other
INTERFACE	Returns interface module in the 5500	ALL
INVERT	Returns status (inverted or normal) of listed parameters TD RD TC RC XC	ALL
INVERT ?	Returns "INVERT xxxxx .. where xxxxx is either 'I' for invert or '.' for noninvert, ordered TD,RD,TC,RC,XC	ALL

Table 4-3. Model 5500 Remote System Commands (Cont.).

COMMAND	FUNCTION	INTERFACE
INVERT xxxxx	Sets status of parameters as shown above.	ALL
LOCK ?	Returns "ALL, RUN/STOP, INJECT, CLEAR, SYNC, RTS/DCD, DTR/DSR, DCE/DTE, RECALL, STORE, SELECT"	ALL
LOCK xx	Locks parameter entered from list above	ALL
LOOP	Returns status of Tx to Rx loop.	ALL
LOOP ?	Returns "OFF, ON"	ALL
LOOP xx	Turns Tx to Rx loop on or off	ALL
LPMODE	Returns status of loop mode	Bell 303 only
LPMODE ?	Returns "SELFTEST, REMOTE"	Bell 303 only
LPMODE xx	Sets status of loop mode as above	Bell 303 only
PROTECT	Sets all protectable parameters to the protect state (This can be undone by using the UNLOCK ALL command described below.)	ALL
RING	Returns ring status	Bell 303 only
RING ?	Returns "Correct Format ====> RING XXX, Where XXX is "ON" or "OFF""	Bell 303 only
RING xxx	Sets ring to on or off	Bell 303 only
RLOCK	Returns status of MSU remote lockout	ALL
RLOCK ?	Returns "ENABLE, DISABLE"	ALL
RLOCK xx	Enables or disables MSU remote lockout	ALL

Table 4-3. Model 5500 Remote System Commands (Cont.).

COMMAND	FUNCTION	INTERFACE
RTS/DCD	Returns status of the RTS/DCD line	Other
RTS/DCD ?	Returns "Either "T" for TRUE or "F" for FALSE"	Other
RTS/DCD x	Sets the RTS/DCD line true or false	Other
RXn	Returns the status of the spare receiver lines where n=Ø, 1, 2, or 3	ALL
SCRNSAV	Returns status of the 5500 screen saver	ALL
SCRNSAV ?	Returns "DISABLE, ENABLE"	ALL
SCRNSAV xx	Enables or disables the screen saver	ALL
SIGQ	Returns status of signal quality	Bell 303 only
SIGQ ?	Returns "Correct Format ====> SIGQ XXX, Where XXX is "ON" or "OFF""	Bell 303 only
SIGQ xxx	Turns signal quality on or off	Bell 303 only
SIM	Returns status of DCE/DTE select	OTHER
SIM ?	Returns "DTE, DCE"	OTHER
SIM xx	Sets DCE/DTE select	OTHER
STATUS	Returns system status as "ROM: PASS, RAM: PASS, USER PROG: PASS, USER PAT: PASS"	ALL
SYNC	Returns sync state	ALL
SYNC ?	Returns ""Either "R" to reset sync loss or "B" to force sync break	ALL
SYNC xx	Sets sync condition as above	ALL

Table 4-3. Model 5500 Remote System Commands (Cont.).

COMMAND	FUNCTION	INTERFACE
TOD	Returns setting of time of day, day of week, and month, date, year as "15:28:11.4 SU Ø3/16/87"	ALL
TOD ?	Returns "Time of Day Format: HH:MM:SS xx MM/DD/YY where xx = SU, MO, TU, WE, TH, FR, or SA"	ALL
TOD xx ...xx	Sets TOD in accordance with format above	ALL
TWEAK	Returns setting of crystal oscillator frequency	ALL
TWEAK ?	Returns "Nominal crystal frequency in Hertz. Must be between 46Ø6ØØØ and 461ØØØØ.	ALL
TWEAK xx	Calibrates crystal oscillator in accordance with format above	ALL
TXn	Returns state of spare transmit lines where n=Ø, 1, 2, 3, 4, or 5	ALL
TXn ?	Returns "Either "T" for TRUE or "F" for FALSE" where n=Ø, 1, 2, 3, 4, or 5	ALL
TXn xx	Sets state of spare transmit lines to true or false where n=Ø, 1, 2, 3, 4, or 5	ALL
UNLOCK ?	Returns "ALL, RUN/STOP, INJECT, CLEAR, SYNC, RTS/DCD, DTR/DSR, DCE/DTE, RECALL, STORE, SELECT	ALL
UNLOCK xx	Unlocks parameters selected from list above.	ALL
VER	Returns Model and version number as "PHOENIX 5500, VERS. 6.ØØ"	ALL

4.9.3.2 Printer Commands

The printer commands are used to control the graph function of the 5500 and to control a printer connected to the Model 5500. Two of these commands, <Control C> and <Control P> are direct action commands. They are used during the print and/or graph operation to exercise direct control over those functions. Entering <Control C> while the printer is printing will cause an interrupt and the printer will stop printing. Entering a <Control P> will remove the interrupt and the printer will return to its printing task.

Since the printer uses a small buffer, 256 bytes, there may be a discontinuity in the output print data when the printer has been interrupted and then restarted; however, the graph function is fully buffered and will not display any discontinuity if it is interrrupted.

Another printer command is the PEND command. This command is used in the ACK-NACK mode to provide a signal to the controller that the 5500 has something to output to the printer. The PEND command uses a four bit flag in the form:

PEND XXXX

For clarity, assigning a number to each position in the flag word gives us:

PEND $X_3X_2X_1X_\emptyset$

This flag word is used by the 5500 to inform the controller if:

$X_\emptyset$ = "1" that the 5500 has a data dump pending.

X_1 = "1" that the 5500 has a data graph pending.

X_2 = "1" that the 5500 has a jitter graph pending.

X_3 = "1" that a key has been pushed on the 5500 that causes a one line printout to occur (ie., pressing error inject will cause the 5500 to output a single line output informing the user that the inject function is on or off). The user may view the current PEND status by entering PEND which will return the flag word.

The user can force a bit in the flag word to a 1 by entering PEND XXXX with X = to 1 or 0. By setting one or more of the bits to a 1, a print dump of that function will be forced. At the completion of a print dump, either forced or controller selected, the controller will set the applicable bits back to zero.

The two remaining printer commands, GRAPH and PRINT involve multiple displays on the remote terminal. These commands will be explained and illustrated on the following pages.

The illustrations and examples on the following pages assume the user has an RS-232 interface module installed. If another interface module is installed in your unit, there may be differences in some of the displays. Normally these differences will appear on those displays that concern test parameters. For example, the graph data selection display, with the RS-232 interface, presents six parameters that may be graphed and/or printed. With the Framed T1 module installed, that same list grows to 12 parameters. However, even though the number of parameters changed, the method of selecting the parameter to be graphed and/or printed remains the same.

To get to the print functions, the PRINT command is entered followed by a <RETURN>:

```
B>PRINT <RETURN>
```

The display will return:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: 1
```

To check the setting of the print enable/disable enter a "1" at the flashing cursor to change the display to:

```
Data printing is now: DISABLED
Enter 'C' to change or <RETURN> to exit: C
```

Entering a "C" will enable printing and change the display to:

```
Data printing is now: ENABLED
Enter 'C' to change or <RETURN> to exit: <RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: 2
```

Entering a 2 will bring up the print conditions and change the display to:

```
The available print conditions are:

(a)  1 MINUTE     (g)  6 HOUR      (m) TEST END
(b)  5 MINUTES    (h) 12 HOURS     (n) SYNC LOSS
(c) 1Ø MINUTES    (i) 24 HOURS     (o) ERR SEC
(d) 15 MINUTES    (j) BIT ERROR    (p) ---------
(e) 3Ø MINUTES    (k) BLOCK ERROR
(f)  1 HOUR       (l) BLOCK

The currently selected conditions are:

(1) 1Ø MINUTES       (2) BLOCK
(3) ----------       (4) ----------

Enter number (1-4) and letter to select or <RETURN> to exit:3o
```

Entering "3o" will add errored seconds as a print condition and change the display to:

```
The available print conditions are:

(a)  1 MINUTE     (g)  6 HOUR      (m) TEST END
(b)  5 MINUTES    (h) 12 HOURS     (n) SYNC LOSS
(c) 1Ø MINUTES    (i) 24 HOURS     (o) ERR SEC
(d) 15 MINUTES    (j) BIT ERROR    (p) ---------
(e) 3Ø MINUTES    (k) BLOCK ERROR
(f)  1 HOUR       (l) BLOCK

The currently selected conditions are:

(1) 1Ø MINUTES      (2) BLOCK
(3) ERR SEC         (4) ----------

Enter number (1-4) and letter to select or <RETURN> to exit:
                                                        <RETURN>
```

Enter <RETURN> and the display returns to:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: 3
```

Enter a "3" to select data types to print and the display changes to:

```
(a)          BIT ERRORS -   (k)            FREQUENCY P
(b)    BIT ERROR RATE -     (l)          POWER LOSSES -
(c)       ELAPSED TIME P    (m)      ERRORED SECONDS P
(d) ELAPSED TIME SECS -     (n)   ERROR FREE SECONDS -
(e)       BLOCK ERRORS P    (o) ERRORED SECOND RATE -
(f)ERRORED BLOCK RATE P     (p)                G821 -
(g)             BLOCKS -    (q)         JITTER FREE -
(h) ERROR FREE BLOCKS -     (r)         JITTER HOLD -
(i)        SYNC LOSSES -    (s)               TIMER P
(j) SYNC LOSS SECONDS P     (t)                BIAS P

"-" means don't print.  "P" means print.
Enter letter to change or <RETURN> to exit: g
```

Enter a "g" to add BLOCKS to the list of parameters to be printed and the display changes to:

```
(a)          BIT ERRORS -   (k)            FREQUENCY P
(b)    BIT ERROR RATE -     (l)          POWER LOSSES -
(c)       ELAPSED TIME P    (m)      ERRORED SECONDS P
(d) ELAPSED TIME SECS -     (n)   ERROR FREE SECONDS -
(e)       BLOCK ERRORS P    (o) ERRORED SECOND RATE -
(f)ERRORED BLOCK RATE P     (p)                G821 -
(g)             BLOCKS P    (q)         JITTER FREE -
```

```
(h) ERROR FREE BLOCKS -   (r)          JITTER HOLD -
(i)       SYNC LOSSES -   (s)                TIMER P
(j) SYNC LOSS SECONDS P   (t)                 BIAS P

"-" means don't print.  "P" means print.
Enter letter to change or <RETURN> to exit: <RETURN>
```

Enter a <RETURN> and the display returns to:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: <RETURN>
```

Enter a <RETURN> to get to the prompt and the prompt returns:

```
B>
```

To setup the graph conditions, enter the GRAPH command followed by a <RETURN>

```
B>GRAPH <RETURN>
```

The display appears as:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 1
```

To check graph enable/disable selection, enter a "1" at the flashing cursor to change the display to:

```
Graph printing is now: DISABLED
Enter 'C' to change or <RETURN> to exit: C
```

Entering a "C" will enable graph printing and change the display to:

```
Graph printing is now: ENABLED
Enter 'C' to change or <RETURN> to exit: <RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 2
```

Entering a "2" will allow the setting of the graph sample resolution and change the display to:

```
Graph sample resolution can be:

(1)  1 SECOND
(2) 1Ø SECONDS
(3)  1 MINUTE
(4) 1Ø MINUTES
(5)  1 HOUR

Current sample resolution is: 1Ø MINUTES
Enter number (1-5) to select or <RETURN> to exit: 3
```

Entering a "3" will select 1 minute for sample resolution and change the display to:

```
Graph sample resolution can be:

(1)  1 SECOND
(2) 1Ø SECONDS
(3)  1 MINUTE
(4) 1Ø MINUTES
(5)  1 HOUR

Current sample resolution is: 1 MINUTE
Enter number (1-5) to select or <RETURN> to exit:<RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 3
```

Entering a "3" permits selection of graph print resolution and changes the display to:

```
Graph print resolution can be:

(3)  1 MINUTE
(4) 1Ø MINUTES
(5)  1 HOUR

Current print resolution is: 1 MINUTE
Enter number (1-5) to select or <RETURN> to exit: 5
```

> ***NOTE***
>
> The print resolution is dependent upon the sample resolution. The print resolution can never be greater then the sample resolution nor can it be more then 2 steps less. Therefore the print resolution display will adjust itself to permit the user to select only the valid print resolution scale dependent upon the setting of the sample resolution.

Entering a "5" will select 1 hour for print resolution and change the display to:

```
Graph print resolution can be:

(3)  1 MINUTE
(4) 1Ø MINUTES
(5)  1 HOUR

Current print resolution is: 1 HOUR
Enter number (1-5) to select or <RETURN> to exit: <RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 4
```

Entering a "4" permits selection of graph data and changes the display to:

```
(a)          BIT ERRORS --
(b)     ERRORED BLOCKS GP
(c)     ERRORED SECONDS G-
(d)   ERROR FREE BLOCKS GP
(e)  ERROR FREE SECONDS G-
(f)        SYNC LOSSES GP

"G-" means graph only, "GP" means graph and print.
Enter letter (a-l) to change or <RETURN> to exit: c
```

Entering a "c" will change errored seconds from graph only to graph and print while the display changes to:

```
(a)          BIT ERRORS --
(b)      ERRORED BLOCKS GP
(c)     ERRORED SECONDS GP
(d)   ERROR FREE BLOCKS GP
(e)  ERROR FREE SECONDS G-
(f)          SYNC LOSSES GP

"G-" means graph only, "GP" means graph and print.
Enter letter (a-l) to change or <RETURN> to exit: <RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: <RETURN>
```

Enter a <RETURN> and the prompt returns:

```
B>
```

4.9.3.3 Event Timing Commands

The event timing commands permit the user to set a timer to record the time between selected intervals. The event timing commands are presented in table 4-4.

Table 4-4. Model 5500 Remote Event Timing Commands

COMMAND	FUNCTION	INTERFACE
ESCALE	Returns scale that the ESTART to ESTOP is measured in	Not T
ESCALE ?	Returns "1US, 1ØUS, .1MS, 1MS, 1ØMS	Not T
ESCALE xx	Sets timer scale to one of the above listed intervals	Not T
ESTART	Returns the event that will start the the timer.	Not T
ESTART ?	Returns "RD/, RD\, TD/, TD\, SQ/, SQ\, DTR/, DTR\, DCD/, DCD\, DSR/, DSR\, CTS/, CTS\, RTS/, RTS\	Not T
ESTART xxx	Selects the event to start the timer from the above list	Not T
ESTOP	Returns the event that will stop the the timer.	Not T
ESTOP ?	Returns "RD/, RD\, TD/, TD\, SQ/, SQ\, DTR/, DTR\, DCD/, DCD\, DSR/, DSR\, CTS/, CTS\, RTS/, RTS\	Not T
ESTOP xxx	Selects the event to stop the timer from the above list	Not T
EVENT	Returns the time between the start and stop events selected by ESTART and ESTOP above. The event time measurement is returned in the units selected by ESCALE above with a maximum resolution of 1 ns. If the event has not occurred, the response will be '-'. If the event exceeds the counter range (4.75 seconds) the response will be OVER. If more than 10 seconds have elapsed since the last event time measurement was made, the response will have an 'I' appended to it indicating inactivity.	Not T

4.9.3.4 User Programs, Patterns, and Sequence Commands

The user programs, patterns, and sequences commands are used to create and store programs and patterns in memory for future use. Table 4-5 presents the user programs and patterns commands. The sequence command (SEQ) is used with the DDS Bell 303 module only and is explained in the Bell 303 option section of this instruction book.

Table 4-5. Model 5500 Remote User Programs and Patterns Commands.

COMMAND	FUNCTION	INTERFACE
RECALL ously stored programs.	Returns locations and names of all	All p r e v i -
RECALL ?	Returns "Select program Ø-9."	All
RECALL x	Recalls the program number as selected by 'x'	All
STORE	Returns locations and names of all previously stored programs.	All
STORE ?	Returns "Form: STORE # '----- name -----' where: # = Ø-9"	All
STORE x'name'	Stores the current program setup in the location specified and with the name assigned	All
USRPAT	Returns the current remote selected user pattern for editing.	All
USRPAT = x	Selects user pattern 1, 2, 3, or 4	All
USRPAT ?	Returns "Enter HEX data separated by spaces. Enter '+' before the data to add it the present pattern. Otherwise, the old pattern is replaced by the new data. Enter '=' followed by 1-4 to change pattern number."	All
USRPAT + xx ... xx	Adds HEX value of xx to current pattern	All
USRPAT xx ... xx	Replaces current pattern with one defined by HEX values of xx.	All

4.9.3.5 BERT Setup Commands

The BERT setup commands are used to configure the 5500 for a particular user application. These commands are of the configuration type in that they are normally entered with a parameter. Table 4-6 presents the BERT setup commands.

Table 4-6. Model 5500 Remote BERT Setup Commands.

COMMAND	FUNCTION	INTERFACE
AUTOSYNC	Returns current status of auto resync function	All
AUTOSYNC ?	Returns "AUTO SYNC FUNCTION FORMAT IS AS FOLLOWS: AUTOSYNC DISABLE AUTOSYNC ENABLE AUTOSYNC TIMED XXX ===> WHERE XXX EQUALS NUMBERS FROM Ø-999 x 1Ø milliseconds."	All
AUTOSYNC xx	Sets auto sync function per above format	All
BIGx	Returns what is displayed on the big bert display { x = 1 or 2 for line 1 (top) or line 2 (bottom)}	All
BIGx ?	Returns "BITS, EMPTY, BE, BER, BLK, BLE, EFB, EBR, TOD, MDY, ET, ED, ETS, ES, EFS, ESR, LOS, SLS, PF, ABE, ABER, CBE, CBER, RBPV, RVR, RVS, RVFS, EFS%, %1sD, FLS, ALRM, AHST"	All
BIGx nnn	Sets big bert display line x to selected parameter nnn	All
BLKS	Returns the number of blocks that will analyzed for this test	All
BLKS ?	Returns "Number of blocks to analyze from Ø to 9999, Ø = continuous."	All
BLKS xx	Sets number of blocks to be analyzed as selected by xx.	All

Table 4-6. Model 5500 Remote BERT Setup Commands (Cont.).

COMMAND	FUNCTION	INTERFACE
BPVRATE	Returns the current bipolar violation error injection rate	T1/T1C
BPVRATE ?	Returns "The injected BPV rate is programable in the form: mE-e where: m= Ø, 1, 2, 3, 4, 5, 6, 7, 8, 9 e = 3, 4, 5, 6, 7"	T1/T1C
BPVRATE mE-e	Sets the BPV inject rate per the above	T1/T1C
BR	Returns current bit rate	Not T
BR ?	Returns "USER, 75, 110, 134.5, 15Ø, 2ØØ, 3ØØ, 6ØØ, 12ØØ, 18ØØ, 24ØØ, 32ØØ, 36ØØ, 48ØØ, 64ØØ, 72ØØ, 8ØØØ, 96ØØ, 14.4K, 16K, 19.2K, 24K, 28.8K, 32K, 48K"	Not T
BR xx	Sets bit rate to value selected by xx as above	Not T
BR	Returns clock rate and source (ie., T1, RX)	T1/T1C
BR ?	Returns "RX, INTERNAL, EXTERNAL JITTER"	T1/T1C
BR xx	Sets clock source as above	T1/T1C
BS	Returns current block size	All
BS ?	Returns "1Ø^3, 1Ø^4, 1Ø^5, 1Ø^6, 1Ø^7, 1Ø^8, 1Ø^9"	All
BS 1Ø^x	Sets block size to selected value per x where x = 3, 4, 5, 6, 7, 8, or 9	All
CLR	This command clears all registers and sets them to zero.	All
CODE	Returns line code setting	T1/T1C
CODE ?	Returns "AMI, B8ZS"	T1/T1C

Table 4-6. Model 5500 Remote BERT Setup Commands (Cont.).

COMMAND	FUNCTION	INTERFACE
CODE xx	Sets line code to AMI or B8ZS	T1/T1C
CS	Returns current character size	Not T
CS ?	Returns "5, 6, 7, 8, CONT"	Not T
CS xx	Sets character size to one of above	Not T
FRAME	Returns current frame state	T1/T1C
FRAME ?	Returns "ENABLE, DISABLE"	T1/T1C
FRAME XX	Enables or disables framing	T1/T1C
FSRC	Returns parameter being measured by frequency counter	All
FSRC ?	Returns "BR, TC, RC, XC"	All
FSRC xx	Selects parameter to be measured by frequency counter	All
INJ	Returns status of error injection	All
INJ ?	Returns "OFF, ON"	All
INJ xx	Turns error injection on or off	All
IRATE	Returns the injected error rate	All
IRATE ?	Returns "The injected error rate is programable in the form: mE-e where: m= Ø, 1, 2, 3, 4, 5, 6, 7, 8, 9 e = 3, 4, 5, 6, 7, 8, 9"	All
IRATE mE-e	Sets the error inject rate per the above	All
MD	Returns current mode	All
MD ?	Returns "ASYNC, SYNC"	Not T
MD ?	Returns "BRIDGE, TERM"	T1/T1C

Table 4-6. Model 5500 Remote BERT Setup Commands (Cont.).

COMMAND	FUNCTION	INTERFACE
MD xx	Sets mode per above	All
PAT	Returns current transmit pattern	All
PAT ?	Returns "63, 511, 2Ø47, REV2Ø47, (2^15)-1, (2^2Ø)-1, QRW, TSET, TRESET, MARK, SPACE, ALT, FOX, SYSY 511, X25 511, USR1, USR2, USR3, USR4"	All
PAT xx	Sets transmit pattern to one of above	All
PR	Returns async parity setting	Not T
PR ?	Returns "NONE, EVEN, ODD"	Not T
PR xx	Sets async parity as above	Not T
RUN	Starts test	All
SB	Returns number of stop bits	Not T
SB	Returns "1, 2"	Not T
SB x	Sets number of stop bits to 1 or 2	Not T
STOP	Stops test	All
TDCLK	Returns clock that is used as DCE mode transmit clocking signal	Not T
TDCLK ?	Returns "TC, XC"	Not T
TDCLK xx	Selects DCE mode transmit clocking signal	Not T

4.9.3.6 BERT Result Commands

The BERT results commands are used to monitor the results of particular BERT functions. In most cases these commands are direct entry commands that do not support a parameter. The exceptions to this will be noted in table 4-7. Table 4-7 lists the BERT results commands.

Table 4-7. Model 5500 Remote BERT Results Commands.

COMMAND	FUNCTION	INTERFACE
ABE	Returns adjusted bit errors.	All
ABER	Returns adjusted bit error rate	All
AHST	Returns alarm history	T1/T1C
ALARM	Returns alarms status	T1/T1C
BA	Returns number of blocks analyzed	All
BE	Returns number of bit errors	All
BER	Returns the bit error rate	All
BIAS	Returns the bias measurement	Not T
BITS	Returns current bit count	All
BLE	Returns number of block errors	All
CBE	Returns number of current bit errors	All
CBER	Returns current bit error rate	All
EBR	Returns errored block rate	All
ED	Returns number of elapsed days since test began	All
EFB	Returns the number of error free blocks	All
EFS%	Returns percent of error free seconds	All
EFS	Returns number of error free seconds	All
ES	Returns number of errored seconds	All
ESR	Returns the errored second rate	All
ET	Returns elapsed time since test began	All

Table 4-7. Model 5500 Remote BERT Results Commands (Cont.).

COMMAND	FUNCTION	INTERFACE
ETS	Returns elapsed time in seconds since test began	All
FLS	Returns number of frame loss seconds	T1/T1C
LOSS	Returns number of sync losses	All
MFREQ	Returns frequency of selected data stream	All
P1sD	Returns percent of one's density	T1/T1C
R/S	Returns run/stop status	All
RBPV	Returns receiver bipolar violations	T1/T1C
RVFS	Returns receiver BPV free seconds	T1/T1C
RVR	Returns receiver BPV rate	T1/T1C
RVS	Returns receiver BPV seconds	T1/T1C
SLS	Returns sync losss seconds	All
TBPV	Returns transmit bipolar violations	T1/T1C
TVFS	Returns transmit BPV free seconds	T1/T1C
TVR	Returns transmit BPV rate	T1/T1C
TVS	Returns transmit BPV seconds	TI/T1C

4.9.3.7 Other Remote Commands

There are other remote commands that are specific to a particular interface module (ie., the high speed jitter commands). These commands are discussed in the option section for the specific interface module.

application note #1

Testing a T-1 Link

1.0 INTRODUCTION

High-speed, T-carrier facilities are gaining momentum. T-carrier systems are those that conform to a series of standards established by AT&T for the formatting of data for transmission at high speeds. These systems include multiplexing equipment, channel service units (CSUs), channel banks, transcoders, and others. This application note covers testing of one of the T-carrier systems, the T-1.

T-1 is the first T-carrier being implemented on a wide scale. T-1 circuits are 1.544Mbps trunk circuits that can be used for voice, data, and video transmission. To transmit an analog voice channel, T-1 equipment digitizes a PAM pulse stream using 8-bit PCM encoding. The PAM samples produce a transmission rate of 64Kbps for each digitized voice channel, compatible with many digital PBXs on the market today.

T-1 testing has become a hot topic for the simple reason companies need to increase their bandwidth capabilities. And communications alternative technologies are often the most cost-effective means of transporting data at very high speeds.

1.1 PURPOSE

The purpose of this application note is to describe typical T-1 testing and the use of the Phoenix Model 5500 Data Communications Analyzer in performing the analysis.

On portions of T-1 circuits implemented using radio, coax, lightwave, or satellite, the data travels as modulation on a carrier frequency. The figures of merit most often used to judge the performance of T-1 circuits include bit error rate (BER) and error free seconds (EFS). At the termination of the T-1 links and on portions of T-1 circuits implemented on T-1 span lines, the signal is transmitted as a digital bipolar waveform. A binary "1" is transmitted as a positive or negative polarity pulse while a "0" (zero) is represented by the absence of a pulse. Each successive "1" is transmitted at the opposite polarity of the one preceeding. This coding rule is called alternate mark inversion (AMI). Bit error analysis is one of the methods used to measure the transmission performance of T-1 lines. In addition to error analysis, the pulse alternation property of bipolar transmission provides a means for testing the lines while in service. This method is refered to as bipolar violation analysis. A bipolar violation occurs whenever the noise and distortion on a span line is high enough to cause a pulse to be missed when it was transmitted or to be detected when no pulse was present. This results in two successive pulses of the same polarity, thus violating the AMI code. Receive bipolar violation rate (RVR) and receive bipolar violation free seconds (RVFS) are the usual measurements which may be performed without interrupting service on the T-1 link.

Digital repeaters are installed on the T1 span line at 6000 foot intervals to regenerate the digital signal. At these regeneration points, the 1544Khz timing signal is stripped off, or recovered, from the bipolar signal. To ensure that this clock is recovered, the bipolar signal must change states before clock signal is lost. AMI-coded signals are restricted to no more than 15 consecutive zeros. Another coding scheme, expected to come into wider use in the future is B8ZS. The Bipolar with 8 Zero Substitution code transmitts a code containing intentional bipolar violations in place of each string of eight consecutive zeros.

T1 data streams are transmitted in both framed and unframed formats. Most private microwave radio link is not required to have framing information. However, all T1 circuits passing through AT&T facilities must contain framing information. The Phoenix 5500 used with the Model 5500-624 Interface Module, provides all the capabilities for total T1 link testing with either D4 framed or unframed data.

NOTE: The Model 5500-624 interface module may also be equipped with the J02 option to allow the testing of T1 lines for high speed jitter in accordance with AT&T specifications.

2.0 T1 LINE TESTING

2.1 BIT ERROR TESTING

The Phoenix Model 5500 is connected as shown in figure 2-1 for bit error analysis of a T1 line. The Phoenix 5500 replaces the T1 multiplexer and/or terminal equipment on one end of the link and the far end is looped back toward the originating end. In this configuration the originating end must operate on a T1 signal with the combined timing jitter of both the transmit and receive paths. If the jitter is excessive it may create link synchronization problems and prohibit loopback testing. In this case full duplex testing should be performed using a second 5500 at the far end.

The 5500 is generally connected to the T1 line through a channel service unit (CSU). The Phoenix 1544 CSU, shown in figure 2-1, provides the proper termination for the T1 circuits, regenerates the T1 signal, and provides remote loopback capability.

The 5500 sends out a T1 SET code to cause the far end CSU to loopback for testing. The 5500 will automatically switch from T1 SET to QRW a few seconds after testing begins. This is to prevent the T1 SET code from being looped back to the near end CSU causing the near end CSU to go into the loopback mode. If the near end CSU goes into the loopback mode, it would remove the 5500 from the test loop. Upon completion of the test, the user should send T1 RESET code to the far end to take the far end CSU out of the loopback mode.

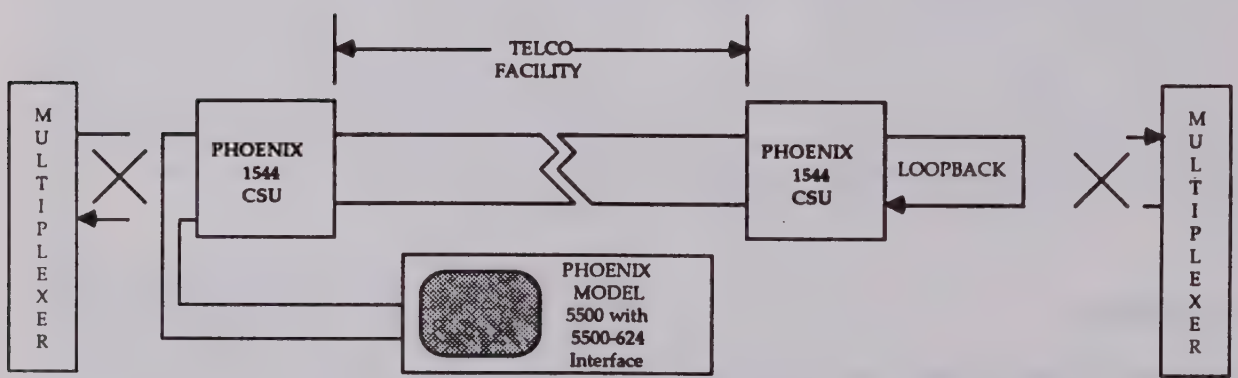


Figure 2-1. T1 BIT Error Testing with Phoenix 5500

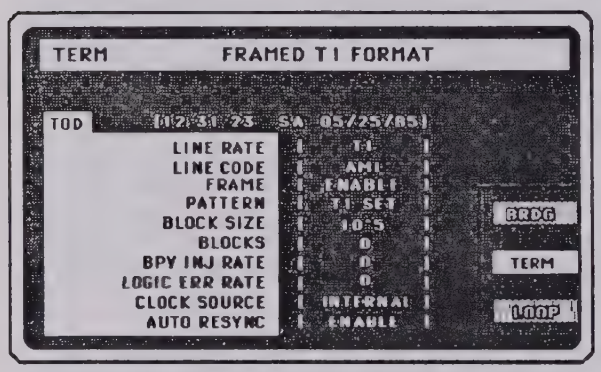
2.1.1 Equipment Required

1 Phoenix Model 5500 Data Communications Analyzer
1 Phoenix Model 5500-624 Interface Module

2.1.2 Equipment Setup

Before applying power to the Model 5500, install the 5500-624 Interface Module. Connect the equipment as shown in figure 2-1.

Turn on the 5500. Depress the **RECALL** switch one time. This will bring the HELP menu to the screen. Enter 6 from the front panel keypad and then press the **GOTO** SoftKey. The FRAMED T1 FORMAT screen should appear as shown below:



Setup the 5500 using this screen as follows:

IMPEDANCE: Using the SoftKey select **TERM**. The **BRDG** (Bridge) position is selected when the 5500 is used as a receive only monitor, and is connected across a terminated T1 line. (Note: Always use the "Bridge" position when connecting the 5500 to a monitor jack.)

TOD: Use the **CURSOR** keys to move the cursor over TOD (Time of Day). Use the **CURSOR** keys to move the cursor over the units in the TOD field. Use the HEX keypad to enter the appropriate alpha/numeric value into the selected parameter.

LINE CODE: Use the **CURSOR** keys to move the cursor over LINE CODE. Use the **SELECT** keys to set the line code to AMI as shown above.

FRAME/UNFRAMED: Use the **CURSOR** keys to move the cursor over FRAME. Use the **SELECT** keys to select ENABLE or DISABLE. For circuits passing through AT&T facilities, select ENABLE. Either ENABLE or DISABLE may be selected for other circuits, depending on circuit requirements.

PATTERN: Use the **CURSOR** keys to move the cursor over PATTERN. Use the **SELECT** keys to set the pattern to T1 SET. This pattern sends out the standard T1 CSU loopback code to cause the remote CSU to loopback for test purposes. After the 5500 begins the test it will revert to QRW. QRW (quasi-random word) is a (2^20)-1 pseudo-random sequence which employs >14 zero suppression and is the prefered pattern for T1 tests.

BLOCK SIZE: Use the **CURSOR** keys to move the cursor over BLOCK SIZE. Use the **SELECT** keys to set the BLOCK SIZE (a 100K block size is recommended for a T1 link test).

BLOCKS: Use the **CURSOR** keys to move the cursor over BLOCKS. Use the **SELECT** keys to set the number of BLOCKS for the test. Normal BER testing of a T1 link requires a minimum of 10^{11} bits be analyzed before printing the final results. At normal error rates, this will require about 18 hours of testing. Selecting "0" permits continous testing.

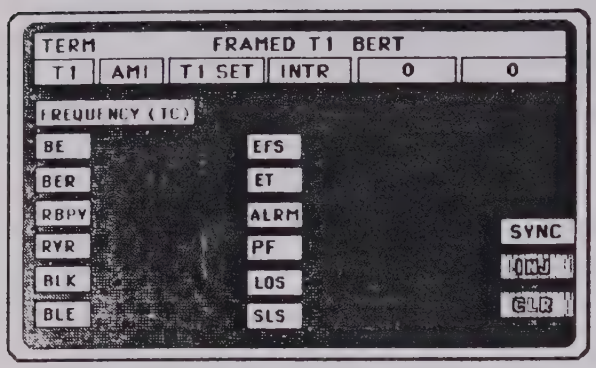
BPV INJ RATE: Use the **CURSOR** keys to move the cursor over BPV INJ RATE. Use the **SELECT** keys to set the BPV INJ RATE to 0. This disables the error inject circuitry which will not be used for BIT Error testing.

LOGIC ERR (INJECT) RATE: Use the **CURSOR** keys to move the cursor over LOGIC ERR RATE. Use the **SELECT** keys to set the LOGIC ERR RATE to 0. The logic errors are what TELCOs call bit errors to distinguish them from BPV errors. Logic errors will not be injected when BIT Error testing is in progress.

CLOCK SOURCE: Use the **CURSOR** keys to move the cursor over CLOCK SOURCE. Use the **SELECT** keys to select INTERNAL. This permits the 5500 to act as the master clock on the T1 line. INTERNAL is always selected when doing loopback testing.

AUTO RESYNC: Use the **CURSOR** keys to move the cursor over AUTO RESYNC. Use the **SELECT** keys to select ENABLE which will allow the 5500 to automatically resynchronize after a synchronization loss.

Press the **MENU** down key one time to select the FRAMED T1 BERT menu as shown below:



This menu will be used to complete the setup of the 5500 for the T1 bit error testing by selecting the parameters the user desires to view during the test. The user may select any 12 of the following parameters for display:

BE = bit errors
BER = bit error rate
BLK = blocks
BLE = errored blocks
EFB = error free blks
TOD= time of day
ET = elapsed test time
ETS = test time in sec
EFS = error free seconds
ESR = error second rate
BITS = recv'd data bits
RVR = Rec BPV rate
RVS = Rec BPV seconds
RVFS = Rec BPV free seconds
LOS = loss of sync
SLS = sync loss seconds
PF = # of power failures
RBPV = rec. BPV'S
EBR = errored blk rate
MDY =month/day/year
ED = errored days
ES = errored seconds
☐ = No parameter display

ALRM = Indicates yellow alarm (B2), signaling frame bit errors (S), loss of PCM (C), and frame bit errors (F). An all dots pattern indicates normal operation on a D4 framed span.

NOTE: Section 4.2 of this instruction book provides full definition of the above parameters.

NOTE: The following choices of parameters for display are for the purpose of demonstrating how to setup the 5500. The operator is free to select any parameters of interest. Also, parameters may be changed at any time during the test without effect on the test being run.

Use the **CURSOR** key to move the cursor over the top left parameter field. Use the **SELECT** key to scroll the parameter list until BE is present. The known generated pattern is compared, bit by bit. Any received bit which does not agree with what is known to have been sent is counted as an error. The error data is accumulated and displayed in this field.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter list until BER appears in the field. This field will now provide a running indication of the health of the circuit under test.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until RBPV appears in the field. This field will provide a count of the receive side bipolar violations.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until RVR appears in the field. This field will keep track of the receive violation rate.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until BLK appears in the field. This field will keep track of the number of blocks received during the test and is composed of all blocks, both errored and error free.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until BLE appears in the field. This field will keep track of the number of blocks received which had at least one bit in error.

Use the **CURSOR** key to move the cursor one position to the right and 5 positions up so that the cursor is on the top right field. Use the **SELECT** key to scroll the parameter field until EFS appears in the field. This field will now indicate the total error free seconds since the start of the test. This parameter is often used as a measure of quality for a T1 line.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until ET appears in the field. This field will then record in hours/minutes/seconds the time since the RUN/STOP switch was set to run and sync was acquired. (ET does not accumulate when the 5500 is not in sync or during sync losses.)

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until ALRM appears in the field.This field will display the alarm staus of the receive side of the circuit. A bit error test on a

circuit with alarms will yield false/invalid results. This field will allow the operator to maintain a watch on the circuit for alarms. (See section 4.2 of this instruction book for a detailed explanation of the ALRM parameter.)

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until PF appears in the field. This field will then record the number of power failures that occur at the 5500 power input during the test.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until LOS appears in the field. This field will keep track of the number of times the bit error rate threshold has been crossed. (Refer to section 4.2 of this instruction book for detailed information on bit error rate threshold.)

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until SLS appears in the field. This field will accumulate the total time the 5500 is out of SYNC.

The setup of the 5500 to perform bit error testing on the T1 data link is now complete.

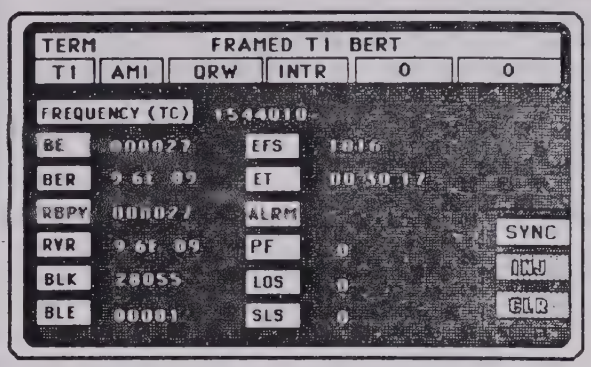
2.1.3 Test Performance

Ensure that the Model 5500 is connected to the near end CSU as shown in figure 2-1. Press the **CLR** softkey to set all the internal counters in the 5500 to zero. Press the **RUN/STOP** switch on the front panel of the 5500. If the remote CSU is appropriately equipped (it will be if it is a Phoenix Model 1544) it will detect the T1 SET code and automatically begin looping data back to the near end. If the far end CSU does not have the automatic loopback feature, a manual patch will have to be made on the far end. Upon successful loopback the 5500 should gain synchronization and begin error analysis. This is indicated by the illumination of the SYNC led on the front panel.

If the SYNC led does not illuminate, recheck all connections and switch settings. (Refer to table 3-2 on (T1) Page 9 in the options section of this instruction book.)

2.1.4 Test Result Evaluation

After the 5500 has obtained sync and begins to collect test data, the operator need only observe the front panel CRT display to begin his analysis of the T1 circuit under test. The display might appear as shown below:



From the above display the following information can be obtained.

The test is presently running (RUN is displayed in upper right corner of display) and the 5500 is in sync (SYNC is indicated on right side of screen opposite softkeys). The T1 SET code has been replaced by the QRW code (second line from the top, between AMI and INTR). The frequency of the internal clock (transmit) is 1.544010MHz.

The test has been running for 30 minutes and 17 seconds (ET parameter).

There have been 1816 error free seconds (EFS parameter) out of a total of 1817 seconds ((30 minutes x 60) + 17).

There have been 27 bit errors (BE parameter) for a bit error rate of 9.6E-09 (BER parameter) and 27 receive bipolar violations (RBPV parameter) for a receive bipolar violation rate of 9.6E-09 (RVR parameter).

During the test time we have received 28,055 blocks (BLK parameter) and one block has had at least one error (BLE parameter).

The power has not failed (PF parameter), there are no alarms (ALRM parameter), and we have not lost sync (LOS and SLS parameters).

AT&T's performance objective is to provide T1 service at 95% error free seconds measured over any 24 hour period. Such a circuit should exhibit a bit error rate less than 10^{-6} when measured over the same time period.

2.2 BIPOLAR VIOLATION MONITORING

Figure 2-2 depicts the proper method to connect the Phoenix 5500 to monitor bipolar violations on a T1 line. In this configuration, the 5500 is connected across the T1 line while live traffic is being transmitted. The 5500 is connected across the line by using the receive monitor jack on the 1544 CSU (most CSU's provide this feature).

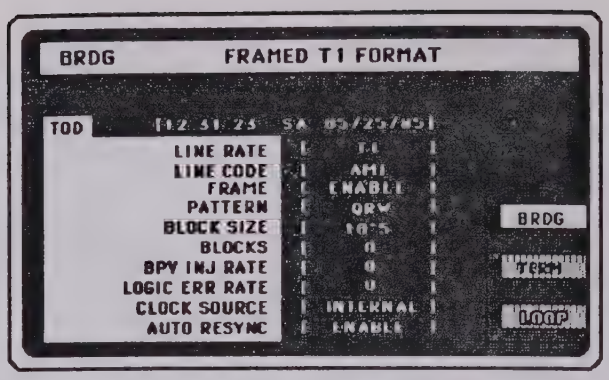
2.2.1 Equipment Required

1 Phoenix Model 5500 Data Communications Analyzer
1 Phoenix Model 5500-624 Interface Module

2.2.2 Equipment Setup

Follow the setup procedures given in section 2.1.2 for the FRAMED T1 FORMAT screen with the following exceptions:

IMPEDANCE: Using the SoftKey select **BRDG.** This allows the 5500 to be connected across the terminated T1 line.



The FRAMED T1 FORMAT screen will appear as above after changing from TERM to BRDG. Press the menu down key one time to select the FRAMED T1 BERT screen. On this menu changes will be made to view parameters that are meaningful to bipolar violation error monitoring.

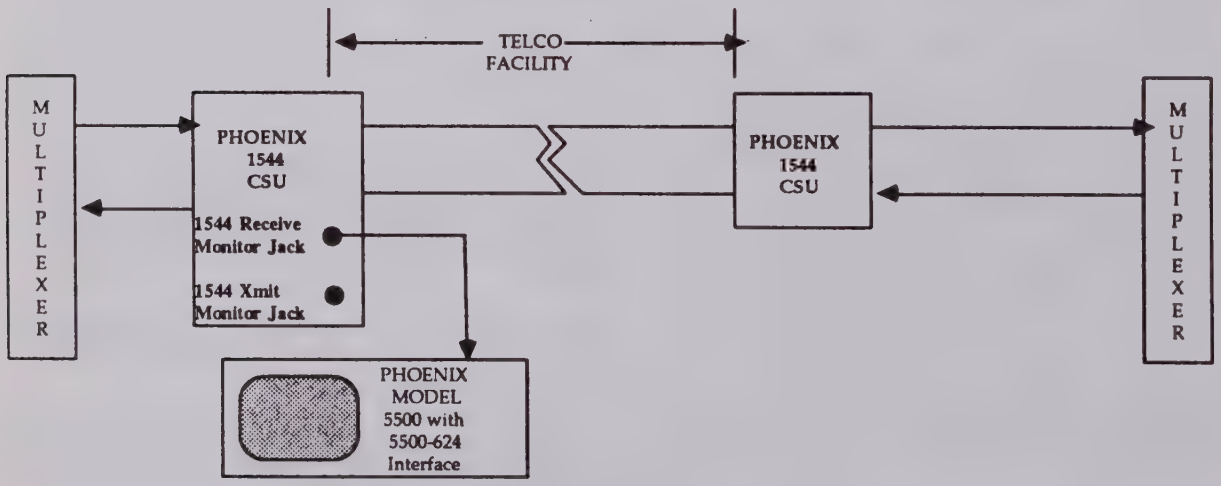
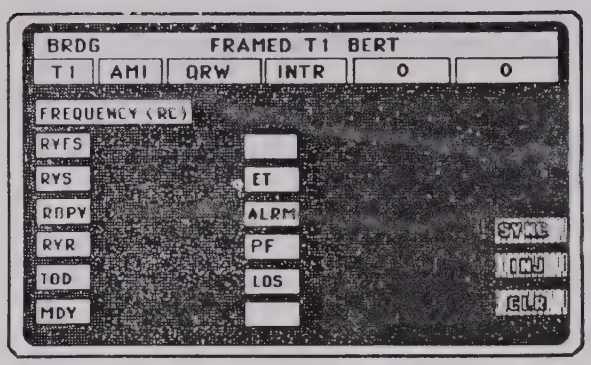


Figure 2-2. T1 Bipolar Violation Monitoring with Phoenix 5500



Observing the top line of the screen it is seen that the change from terminate to bridge that was made on the previous screen is reflected on this screen in the upper left corner.

Use the **CURSOR** key to move the cusor over the top left field. Use the **SELECT** key to scroll the parameter field until RVFS appears in this field. This field will provide a count of the number of seconds in which no violations occured on the receive pair of the T1 line under test.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECET** key to scroll the parameter field until RVS appears in the field. This field will provide a count of each second in which at least one receive violation occurs.

Use the **CURSOR** key to move down three fields (RBPV and RVR should still be set from the previous setup). Use the **SELECT** key to scroll the parameter field until TOD appears in the field. This parameter is a time-of-day clock which shows the time in hours, minutes, and seconds. It is most useful when operating the 5500 with a printer as the exact time is then printed on the test results for future reference.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until MDY appears in the field. This field will present the month, day, and year. This parameter is generally used with TOD to imprint the printer output for indentification.

Use the **CURSOR** key to move the cursor one field to the right. Use the **SELECT** key to scroll the parameter field to ☐ (blank). Use the **CURSOR** key to move the cursor to the top right parameter field. Use the **SELECT** key to scroll the parameter field to ☐ (blank). The screen should now appear as shown above and the 5500 is ready to begin bipolar violation monitoring.

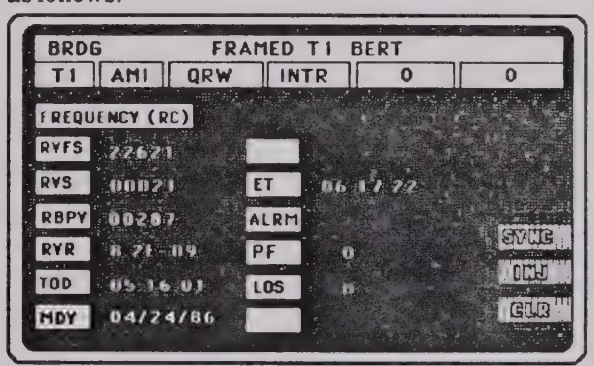
2.2.3 Test Performance

Ensure that the Model 5500 is connected to the near end CSU as shown in figure 2-2. Press the **CLR** softkey to set all the internal counters in the 5500 to zero. Press the **RUN/STOP** switch on the front panel of the 5500. The 5500 should gain synchronization and begin tracking bipolar violations. This is indicated by the illumination of the SYNC led on the front panel.

If the SYNC led does not illuminate, recheck all connections and switch settings. (Refer to table 3-2 on (T1) Page 9 in the options section of this instruction book.)

2.2.4 Test Result Evaluation

After the test period has been completed, or for that matter, at any time during the test, the operator may observe the 5500 CRT display to evaluate the performance of the T1 link under analysis. At this time the display might appear as follows:



From the above display the following information can be obtained.

The test has been completed (RUN is no longer displayed in upper right corner of the display) and the 5500 is no longer in sync (SYNC light on front panel is off and SYNC appears half intensity on display).

The test ran for 6 hours, 17 minutes and 22 seconds (ET parameter).

The current date is April 24, 1986 (MDY parameter) and the current time is 5:16:01 AM (TOD parameter).

Neither sync nor power was lost during the test (LOS and PF parameters).

During the time of the test there were 22,621 seconds in which there were no errors (RVFS parameter). There were 21 seconds in which at least one error occured (RVS parameter).

There were a total of 287 bipolar violations on the receive line during the test (RBPV parameter) which worked out to a 8.2E-9 receive violation rate (RVR parameter).

User Notes

5500 Data Communications Analyzer

Phoenix microsystems

Phoenix Instruction Book

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5.1 GENERAL

The Model 5500 Data Communications Analyzer is a high speed test set composed of a chassis, power supply, and four printed circuit boards. The four PC boards are the 5500 control board, video control board, front panel display/keypad board, and an interface board. The interface board may be one of several plug-in modules, allowing the 5500 to operate in a variety of configurations.

Each 5500 is supplied with a 9V NI-CAD battery and necessary control logic to back up the read/write memory during power down.

5.2 ADJUSTMENTS

5.2.1 Video Intensity Adjustment

The 6.00 revision and up of the Model 5500 software uses a different cursor highlighting mode than has been used in the past. Previously the cursor was identified by an inverse field with black alphanumerics. To improve the visibility of the cursor it is now an inverse field with double intensity alphanumerics. Since this change uses components that are not used in previous software editions, it may be necessary to adjust the intensity of the cursor alphanumerics when installing software revision 6.00.

The following steps should be followed to adjust the cursor intensity:

1. Refer to figure 5-1. Remove the bottom cover from the Model 5500 and locate the video board.

2. Turn on the Model 5500 and observe the CRT display.

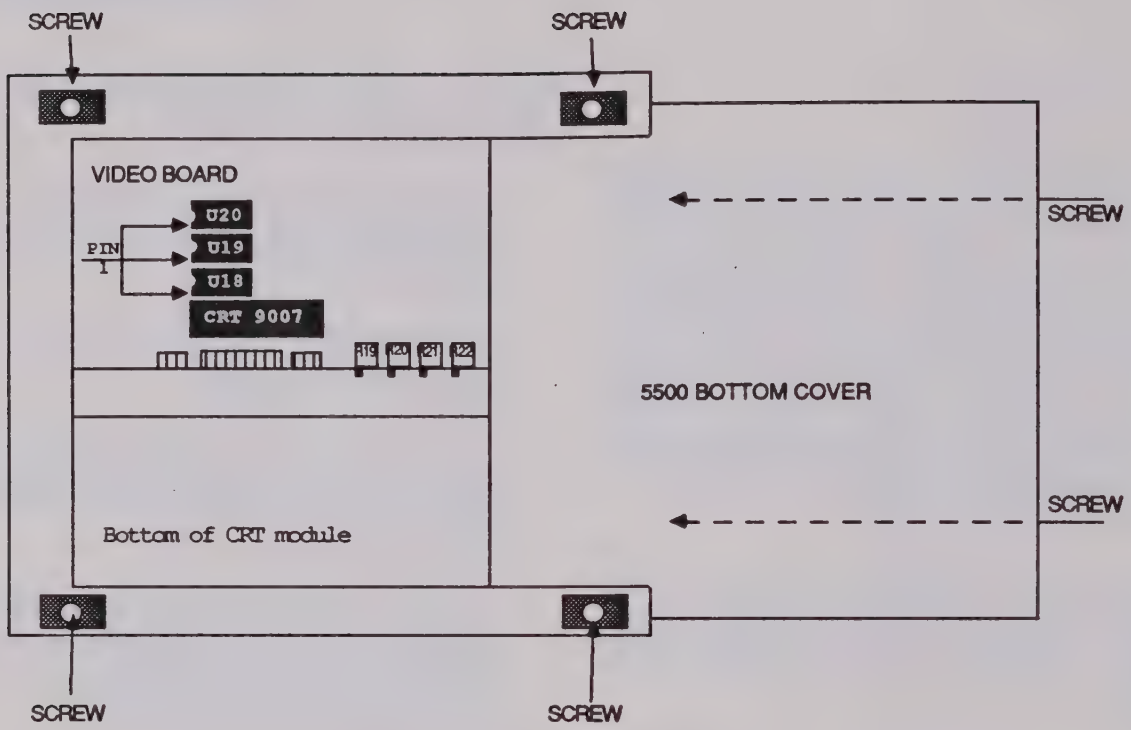
3. Locate R19 and adjust it until the intensity of the cursor alphanumerics appear to be double bright.

4. If you are going to use an external monitor with your 5500 proceed with step 5. If you are not going to use an external monitor go to step 7.

5. Connect the external monitor to the video out jack on the rear panel of the Model 5500.

6. Locate R21 and adjust it until the intensity of the cursor alphanumerics appear to be double bright.

7. Replace the bottom cover of the Model 5500 and return the unit to service.



1. Place the Model 5500 upside down on a clean surface.

2. Remove the six screws shown in the figure above and slide the bottom cover back to gain access to the video board.

View of Video Board in Model 5500
Figure 5-1

5.2.2 PROM Replacement

When it becomes necessary or desired to update your Model 5500 to a different software revision level, it will be necessary to remove and replace the PROM chips in your unit with PROMs which contain the new software. The Model 5500 uses up to six PROMs (depending on software revision level). Three PROMs (U55, U56, and U57) are located on the control board and the remaining three (U18, U19, and U20) are located on the video board. To replace the PROMs, follow the steps below:

1. Refer to figure 5-2. Remove the top cover from the 5500 to gain access to the control board.

2. Locate U55, U56, and U57 on the top of the control board.

3. Remove the existing PROMS (U55, U56, U57) from their sockets.

4. Locate PROM U55 in the shipping container and insert it into the U55 socket. Insure that the notch faces towards the front of the 5500.

5. Locate PROM U56 in the shipping container and insert it into the U56 socket. Insure that the notch faces towards the front of the 5500.

6. Locate PROM U57 in the shipping container and insert it into the U57 socket. Insure that the notch faces towards the front of the 5500.

7. Turn the 5500 over. Refer to figure 5-1. Remove the bottom cover to gain access to the the Video Board.

8. Locate and remove PROMs U18, U19, and U20 on the top of the control board. (Note: not all 5500s will have all three PROMs installed - some may have only U18 installed.)

9. Locate PROM U18 in the shipping container and insert it into the U18 socket. Insure that the notch faces towards the front of the 5500.

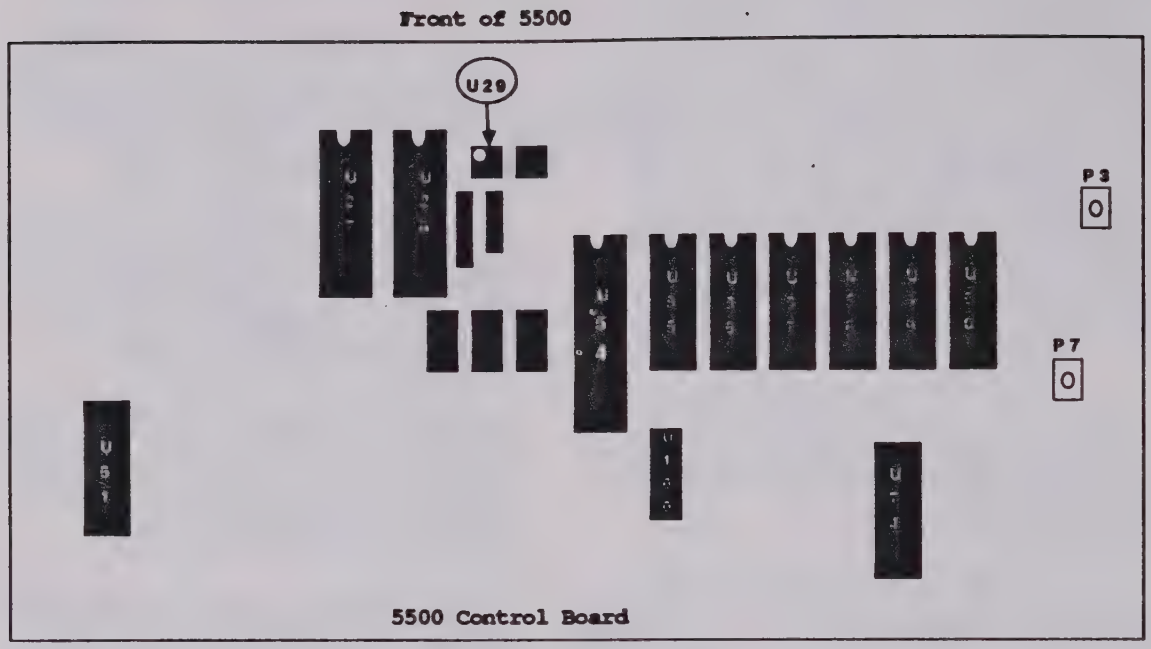
10. Locate PROM U19 in the shipping container and insert it into the U19 socket. Insure that the notch faces towards the front of the 5500.

11. Locate PROM U20 in the shipping container and insert it into the U20 socket. Insure that the notch faces towards the front of the 5500.

12. To maintain your warranty, place the removed PROMs into the container that held the new PROMs and return them, along with the serial number of the 5500 into which the new PROMs were installed, to:

Customer Service Manager
PROM Return
Phoenix microsystems. inc.
991 Discovery Drive
Huntsville, AL 35806

The Model 5500 is now ready for service. However, the cursor intensity may have to be adjusted. Before replacing the bottom cover, turn the 5500 on and check the video intensity levels (pay particular attention to the cursor intensity. If the intensity levels are not correct, follow the procedure given in the intensity adjustment procedure, paragraph 5.2.1 above. If the intensity does not require adjustment, replace the top and bottom covers and return the 5500 to service.



NOTES:

1. Always insure that IC's are replaced with pin one in pin one's socket.
2. U55, 56, and 57 are program ROMs, U58, 59, 60 are RAMs.
3. U29 Non-volitile RAM.

View of Control Card in Model 5500
Figure 5-2

5.2.3 TWEAK Adjustment

The following procedure should be followed when making the TWEAK calibration adjustment as described in table 4-3 of this manual.

1.Place the 5500 power switch to the "OFF" position.

2. Remove the top cover of the 5500 by removing the two top cover screws at the rear of the unit.

3. Place the 5500 power switch to the "ON" position.

4.Connect the terminal to 5500 remote port with an RS-232C cable.

5. Press the RECALL switch on the 5500 front panel.

6. Press 2 on the front panel keypad (to select the remote configuration menu).

7. Press the GO TO softkey to activate the remote configuration menu.

8. Use the remote configuration menu to match the 5500 to the terminal in use. Select RS-232 and CR-LF.

9. Connect a frequency counter to pin 15 of U87 (refer to figure 5-3).

NOTE: Use a HP Model 5315B (with option 4) frequency counter or equivalent. (Option 4 is a temperature compensated crystal for increased accuracy.)

10. Connect the frequency counter ground to signal ground test point as shown in figure 5-3.

11. Type TWEAK (space) XXXXXXX (where xxxxxxx = seven (7) digits displayed on the frequency counter.)

12. The zero offset in the frequency reading has now been removed from the frequency counter in the 5500.

13. Replace the bottom cover and return the 5500 to service.

5.2.4 Sync Loss Threshold

In order to change the sync loss threshold it is necessary to remove the top cover from the Model 5500. Remove the two Phillips head screws in the rear top cover retaining rail and slide the cover out the back. Located above the CRT on the main control board between IC's U20 and U35 is a 14 pin header with jumper straps on it (refer to figure 5-4). The jumper straps control the sync loss criteria as described below.

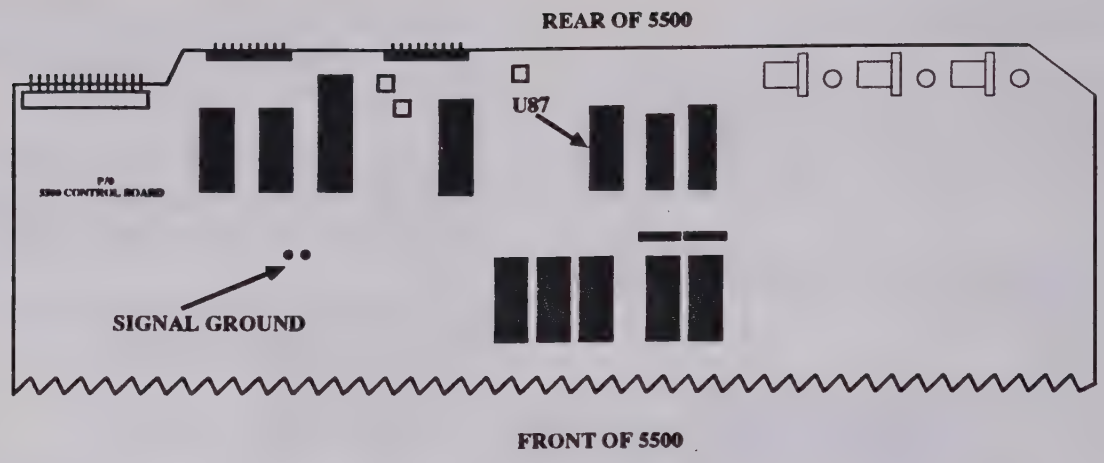
SYNC LOSS CRITERIA

1. X, Y, and Z must be high.

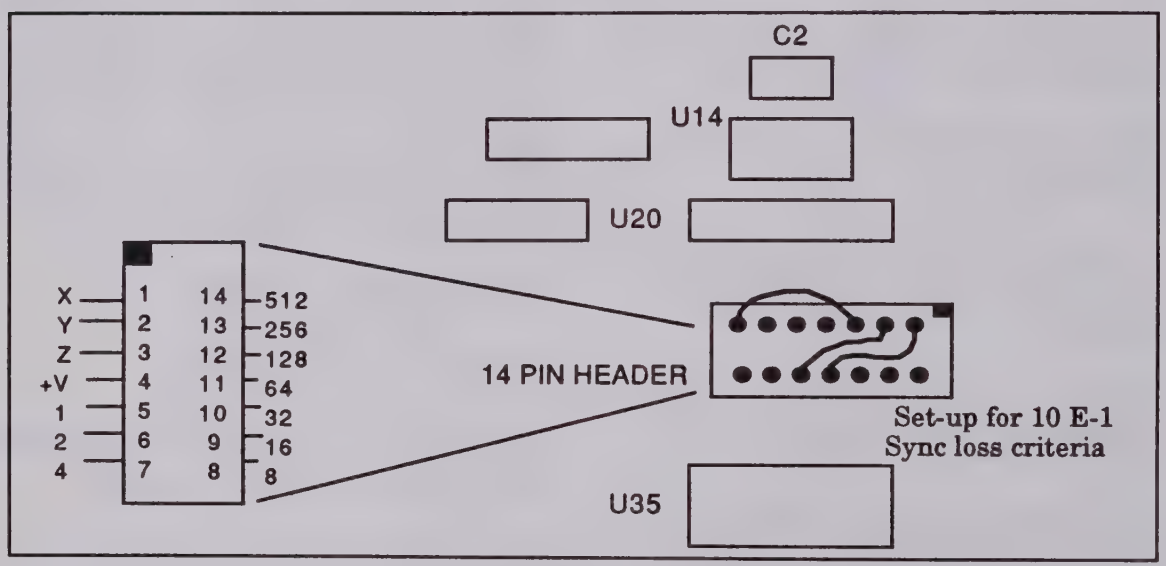
2. 1, 2, 4, 8, 16, 32, 128, 256, and 512 are the outputs of the bit error counter.

3. Patch the bit error outputs to X, Y, and Z as desired to select a count/thousand bits. Only one output at a time may be patched to X, Y, or Z.

4. EXAMPLE 1: (as shipped from factory)
X to 64 (pin 1 strapped to pin 11)
Y to 32 (pin 2 strapped to pin 10)
Z to 4 (pin 3 strapped to pin 7)
X+Y+Z=1 64+32+4 = 100 errors/thousand bits or BER = 10-1



TWEAK Adjustment Locations
Figure 5-3



Sync Threshold Adjustment Location
Figure 5-4

5. EXAMPLE 2:
X = 128 (pin 1 strapped to pin 12)
Y = 64 (pin 2 strapped to pin 11)
Z = 8 (pin 3 strapped to pin 8)
X+Y+Z = 64+32+8 = 200 errors/thousand bits or BER = 2x10-1

6. EXAMPLE 3:
X = 1 (pin 1 strapped to pin 5)
Y = +V (pin 2 strapped to pin 4)
Z = +V (pin 3 strapped to pin 4)
X+Y+Z = 1+0+0 = 1 error/1000 bits.

This connection sets the minimum BER threshold for a sync loss at $1x10^{-3}$.

The sync loss threshold can be varied from $8.96x10^{-1}$ errors/bit to $1x10^{-3}$ errors/bit. A loss of sync is also counted if data transitions do not occur for more than two seconds.

5500
Data Communications Analyzer

Phoenix
microsystems

options

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Model 5500-300 CCITT V.35
Model 5500-450 RS-449/MIL-188C-114
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Model 5500-555 MSU I/O Control Module
Model 5500-600 DS1/DS1C
Model 5500-624 DS1 (T1)
Model 5500-628 ESF (T1)
Model 5500-700 T-2
Model 5500-805 CCITT G.703 8.448 Mbps
Model 5500-810 CCITT G.703 64 Kbps
Model 5500-815 CCITT G.703 2.048 Mbps
Model 5500-900 Bell 303
Model 5500-J01 Low Speed Jitter Option
Model 5500-J02 High Speed Jitter (T1) Option
Model 5501 G821 Performance Evaluation

Model 5500-200

RS-232C Interface Module

1.0 INTRODUCTION

This section details the operation of the Model 5500-200 RS-232 Interface Module option. The logic required to operate in SYNC and ASYNC mode is located within the Model 5500 itself, therefore the interface module performs only the mechanical and electrical interfacing of the EIA RS-232 standard signals to the TTL level signals used within the Model 5500. DCE or DTE emulation, and SYNC or ASYNC mode operation are controlled and switchable from the Model 5500 front panel keys, or by commands over the remote ports.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-200 RS-232 Interface Module specifications.

Table 2-1. Model 5500-200 Specifications

CHARACTERISTIC	SPECIFICATION
Modes	Synchronous or Asynchronous
Emulation	DCE or DTE
Data Rates	50 bps to 20.0 kbps per EIA RS-232C
Character Size	5, 6, 7, 8 data bits
Parity	Odd, Even, or no parity bit
Stop Bits	1 or 2 bits
Input Data Characteristics	Mark signal, binary state 1, or OFF = -3 Volts Min.
	SPACE signal, binary state 0, or ON = +3 Volts Min.
Line Drivers	Output Voltage: Selection of ±5.5 ±.5V peak for worst case MODEM testing or ±9.0 ±2.0V peak for normal BER testing. Selection is made by strap options on the RS-232 interface module.
	Factory set for nominal ±9.0 V. ±2.0 V. operation.
	Output Impedance: 300 ohms minimum
	Slew Rate: 30.0 volts per microsecond maximum.
	Short-circuit Current: 12 milliamps maximum.

Table 2-1. Model 5500-200 Specifications (Cont)

CHARACTERISTIC	SPECIFICATION
Line Receiver	Maximum Input Voltage: ± 25 Volts
	Load Impedance: 3000 ohms min. to 7000 ohms max.
	MARK Voltage: 0.0 Volts Max.
	SPACE Voltage: 2.0 Volts Min.

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-200 RS-232C interface is capable of operation in Synchronous and Asynchronous modes with both DCE and DTE configuration. The module has two 25 pin subminiature 'D' type connectors; normally Male for DCE and Female for DTE. In addition, the DCE/DTE emulation is electronically switchable from the Model 5500 front panel or via command over either remote control port. Figure 2-1 presents a simplified block diagram of the Model 5500-200 module. Table 2-2 presents the RS-232 connector pin assignments.

3.0 OPERATION

3.1 DATA TERMINAL EQUIPMENT (DTE) CONFIGURATION

The Model 5500 may be configured as Data Terminal Equipment (DTE) for testing Data Communications Equipment (DCE) such as Modems, Multiplexers, or other peripheral equipments configured as DCE. This is accomplished by toggling the front panel key labeled 'DCE/DTE' until DTE appears in the upper left hand corner of the BERT CRT display (refer to section 3.2 of this instruction book for location and description of the Model 5500 controls and indicators). In the synchronous mode of operation the Model 5500 maybe set to derive clock from the equipment under test or it may generate the clock internally and provide it to the equipment under test.

In the asynchronous mode of operation, data is transmitted and received without a clock. Start and stop bits provide proper decoding of the data bits in each character (byte) sent while timing is extracted from the bit transition. In Synchronous operation, with the DCE under test acting as the source of timing, the Model 5500 bit rate selection should be set to EXTERNAL. In this position the Model 5500 will derive clock from pin 15 (Transmission signal Element timing-DCE Source) of the DTE I/O connector on the interface module. Transmit data and clock are available on pins 2 and 24 respectively, and receive data and clock are available on pins 3 and 17 respectively.

If a Bit Rate is selected on the Model 5500 then the internal generator of the test set supplies the clock signal to the equipment under test. If the user desires to test at a non-standard bit rate the unit can also be operated with an externally applied USER CLOCK into the rear panel BNC connector with the Model 5500 Bit Rate field set to USER. The frequency of this externally applied clock is read on the CRT display by scrolling through the frequency selections to the appropriate option-either TC or BR.

In either case the test set ignores signals present on pin 15 of the I/O connector. Transmit data and clock are on pins 2 and 24. Receive data and clock are on pins 3 and 17, respectively.

When operated in an Asynchronous mode the Model 5500 bit rates are internally generated. The appropriate character size, number of stop bits, and parity must also be selected using the front panel cursor and select keys. In this mode of operation no clock signals are transmitted. Transmit data appears on pin 2 and Receive data on pin 3 of the I/O connector. Any signals appearing on pins 15 and 17 are ignored. The Model 5500 recovers clock from the received data transitions to provide internal synchronization to the received patterns.

3.1.1 Controls and Indicators

Model 5500 front panel keys labeled RTS/DCD and DTR/DSR enable the user to turn RTS and DTR ON and OFF when the Model 5500 is configured as a DTE.

Table 2-2. RS-232 Connector Pin Assignments

Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
					From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	AA	101	Protective Ground	X						
2	BA	103	Transmitted Data			X				
3	BB	104	Received Data		X					
4	CA	105	Request to Send					X		
5	CB	106	Clear to Send				X			
6	CC	107	Data Set Ready				X			
7	AB	102	Signal Ground (Common Return)	X						
8	CF	109	Received Line Signal Detector				X			
9			(Reserved for Data Set Testing)							
10			(Reserved for Data Set Testing)							
11			Unassigned							
12	SCF	122	Sec. Rec'd. Line Signal Detector				X			
13	SCB	121	Sec. Clear to Send				X			
14	SBA	118	Secondary Transmitted Data			X				
15	DB	114	Sig. Element Timing (DCE Source)						X	
16	SBB	119	Secondary Received Data		X					
17	DD	115	Rec. Sig. Element Timing (DCE Source)						X	
18			Unassigned							
19	SCA	120	Secondary Request to Send					X		
20	CD	108.2	Data Terminal Ready					X		
21	CG	110	Signal Quality Detector				X			
22	CE	125	Ring Indicator				X			
23	CH/CI	111/112	Data Signal Rate Selector (DTE/DCE Source)				X	X		
24	DA	113	Xmit. Sig. Element Timing (DTE Source)							X
25			Unassigned							

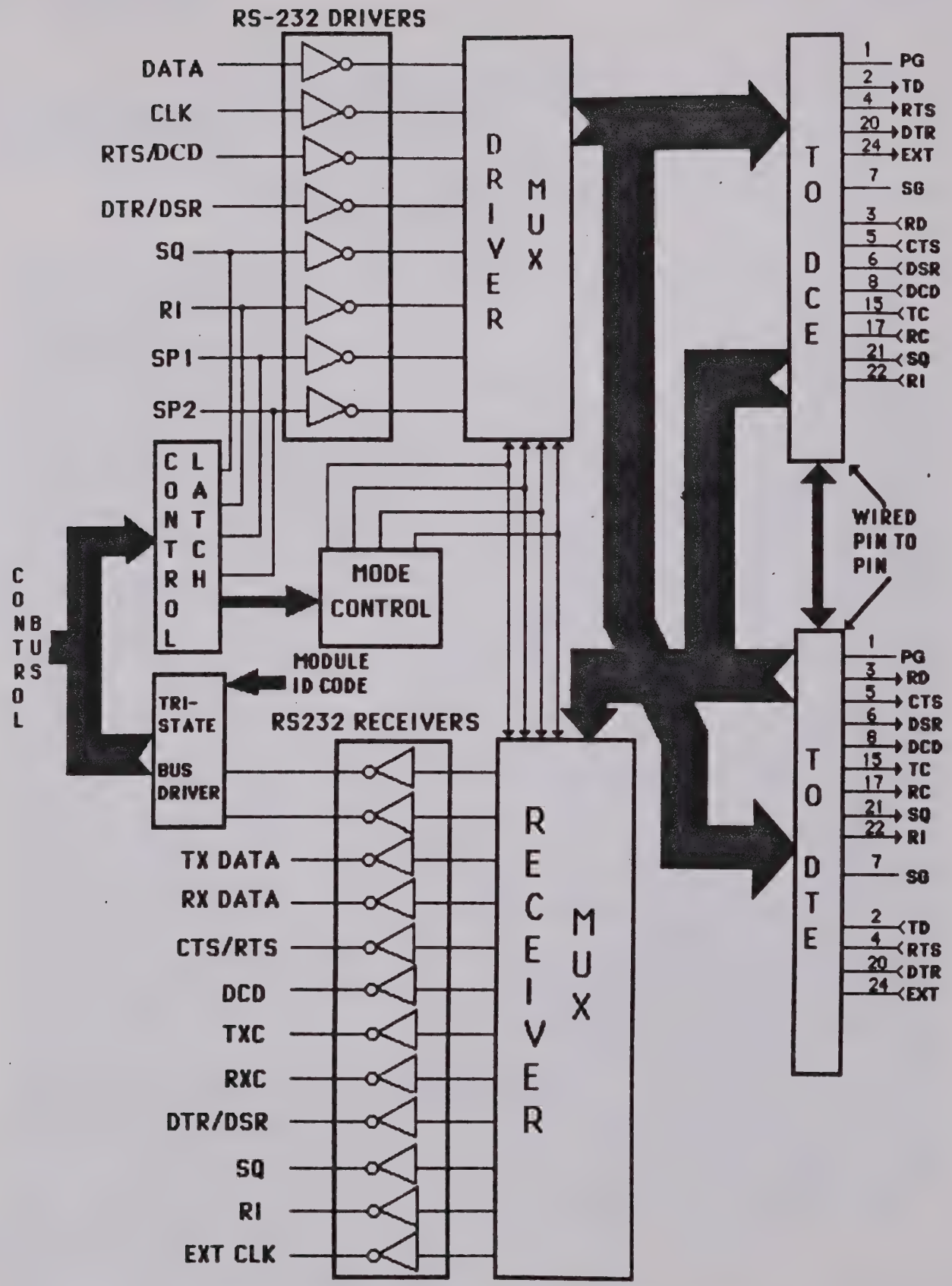

Figure 2-1. Model 5500-200 RS-232C Interface Module Block Diagram

Twelve green LED's provide visual indication of the primary lead status as follows:

Transmit Data - (TD)
Receive Data - (RD)
Transmit Clock - (TC)
Receive Clock - (RC)
Request to Send - (RTS)
Clear to Send - (CTS)
Data Set Ready - (DSR)
Data Terminal Ready - (DTR)
Data Carrier Detect - (DCD)
Ring Indication - (RI)
Signal Quality - (SQ)
Transmit Clock External - (SCTE).

The front panel key labeled DCE/DTE electronically switches the rear panel I/O Connector functions from DCE to DTE and vice versa. This eliminates the need for special cables to use with the RS-232 interface module. These and any other functions, and indications may accomplished and displayed at a remote terminal using the RS-232 or IEEE-488 remote control ports.

3.2 DATA COMMUNICATIONS EQUIPMENT (DCE) CONFIGURATION

The Model 5500 may also be configured to operate as a DCE by toggling the DCE/DTE front panel key until the DCE indication appears in the upper left hand corner of the CRT display. Again, either synchronous or asynchronous peripherals can be tested as in the DTE configuration.

In synchronous mode, the Model 5500 may derive clock from the DTE under test or supply clock to the equipment from its own internal generator. When set to EXTERNAL CLOCK, the Model 5500 receives timing from the DTE Transmit Signal Element Timing on pin 24 of the rear panel DTE I/O connector. The frequency of the external clock is read on the CRT display by scrolling through the frequency selections to XC. Under this condition the Transmit Data on pin 2 and Transmit Signal Element timing on pin 24 are analyzed by the model 5500.

The Model 5500 generates Receive Data on pin 3 and Receive Signal Element timing on pin 17 in accordance with the DTE supplied clock on pin 24.

If it is desired to have the Model 5500 supply clock for the equipment under test it is necessary to select the desired bit rate instead of EXTERNAL. In this case, the model 5500 supplies timing to the DTE under test on pin 15 of the I/O connector. The Model 5500 analyzes the Transmit Data on pin 2 and Transmit signal timing on pin15. Receive Data on pin 3 and Receive Signal Element timing on pin 17 are generated from the Model 5500 internal clock source. A user supplied external clock signal into the USER CLOCK BNC jack will cause the Model 5500 to generate data and clock at the externally applied clock rate when the Mqdel 5500 is set to USER in the BIT RATE field.

Asynchronous DCE mode operation of the Model 5500 requires selection of the ASYNC mode, bit rate, character size, parity, and number of stop bits. Data is generated and received in character format with no clock signals provided.

Timing is derived from the data transitions and the start and stop bits location identifies the data (character) and parity bits to the receiver for proper decoding.

3.2.1 Controls and Indicators

Front panels keys are available which enable the user to turn Data Set Ready (DSR) and Data Carrier Detect (DCD) "ON" and "OFF" in the DCE mode operation. In addition, these conditions, and any other settings can also be controlled from a remote terminal using the RS-232 or IEEE-488 rear panel remote control ports.

The twelve green LED indicators provide status of the primary interface signal leads as discussed earlier in section 3.1.1.

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Model 5500-300

CCITT V.35 Interface Module

1.0 INTRODUCTION

The Model 5500-300 CCITT V.35 Interface Module option is designed to permit the Model 5500 to be configured to test both DCE and DTE devices. This CCITT Recommendation (V.35) covers data exchanged in a serial format with a synchronous clock in a balanced mode. The cable lengths usable with the V.35 interface decreases sharply as the data rate increases and while it may be possible to operate at rates up to 7 Mbps, the cable between test set and device should be kept as short as possible at these rates.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-300 CCITT V.35 Interface Module specifications. Table 2-2 presents the connector pin assignments.

2.1 FUNCTIONAL DESCRIPTION

A block diagram of the V.35 interface module is presented in figure 2-1. The DCE and DTE I/O connectors provide the mechanical interface between the Model 5500 and the equipment under test. The DCE is male and DTE is a female connector.

Table 2-1. Model 5500-300 Specifications

CHARACTERISTIC	SPECIFICATION
Mode	Synchronous
Emulation	DCE or DTE
Data Rate	7 MHZ maximum (dependent upon cable length).
Balanced Drivers	Terminal-to-Terminal
Voltage Swing	4 . 0 Volts ± 20% into a 100 ohm resistive load.
	Source Impedance: 100 ±10% ohms
	Rise Time: Less than 40 nsec
Balanced Receivers	Load Impedance: 100 ±10% ohms
	Resistance between shorted terminals to ground: 150 ± 10%ohms.
Unbalanced Drivers (RS-232 C/V.28)	Output Voltage: ±9.0 ±2.0 v. peak
	Output Impedance: 300ohms minimum
	Slew Rate: 30.0 volts per microsecond maximum.
	Short Circuit Current: 12maximum.

Table 2-1. Model 5500-300 Specifications (Cont)

CHARACTERISTIC	SPECIFICATION
Unbalanced Receivers (RS-232C/V.28)	MARK Voltage: -5.0 volts maximum SPACE Voltage: +5.0 volts minimum Maximum Input Voltage: ±25 Volts Load Impedance: 3000 to 7000 ohms MARK Voltage: 0.0 volts maximum SPACE Voltage: 2.0 volts minimum

Table 2-2. Connector Pin Assignments

PIN	CIRCUIT	DESCRIPTION
A	AA	PROTECTIVE GROUND
B	AB	SIGNAL GROUND
C	CA	REQUEST TO SENT
D	CB	CLEAR TO SEND
E	CC	DATA SET READY
F	CF	RECEIVED LINE SIGNAL DETECTOR
H	CD	DATA TERMINAL READY
J	CE	RING INDICATOR
K	-	LOCAL TEST
L		UNASSIGNED
M		UNASSIGNED
N		UNASSIGNED
P	SD (A)	SEND DATA
R	RD (A)	RECEIVED DATA
S	SD (B)	SEND DATA
T	RD (B)	RECEIVED DATA
U	SCTE (A)	SERIAL CLOCK TRANSMIT EXTERNAL
V	SCR (A)	SERIAL CLOCK RECEIVE
W	SCTE (B)	SERIAL CLOCK TRANSMIT EXTERNAL
X	SCR (B)	SERIAL CLOCK RECEIVE
Y	SCT (A)	SERIAL CLOCK TRANSMIT
Z		
AA	SCT (B)	SERIAL CLOCK TRANSMIT
BB		
CC		SPARE
DD		UNASSIGNED
EE		SPARE SIGNAL

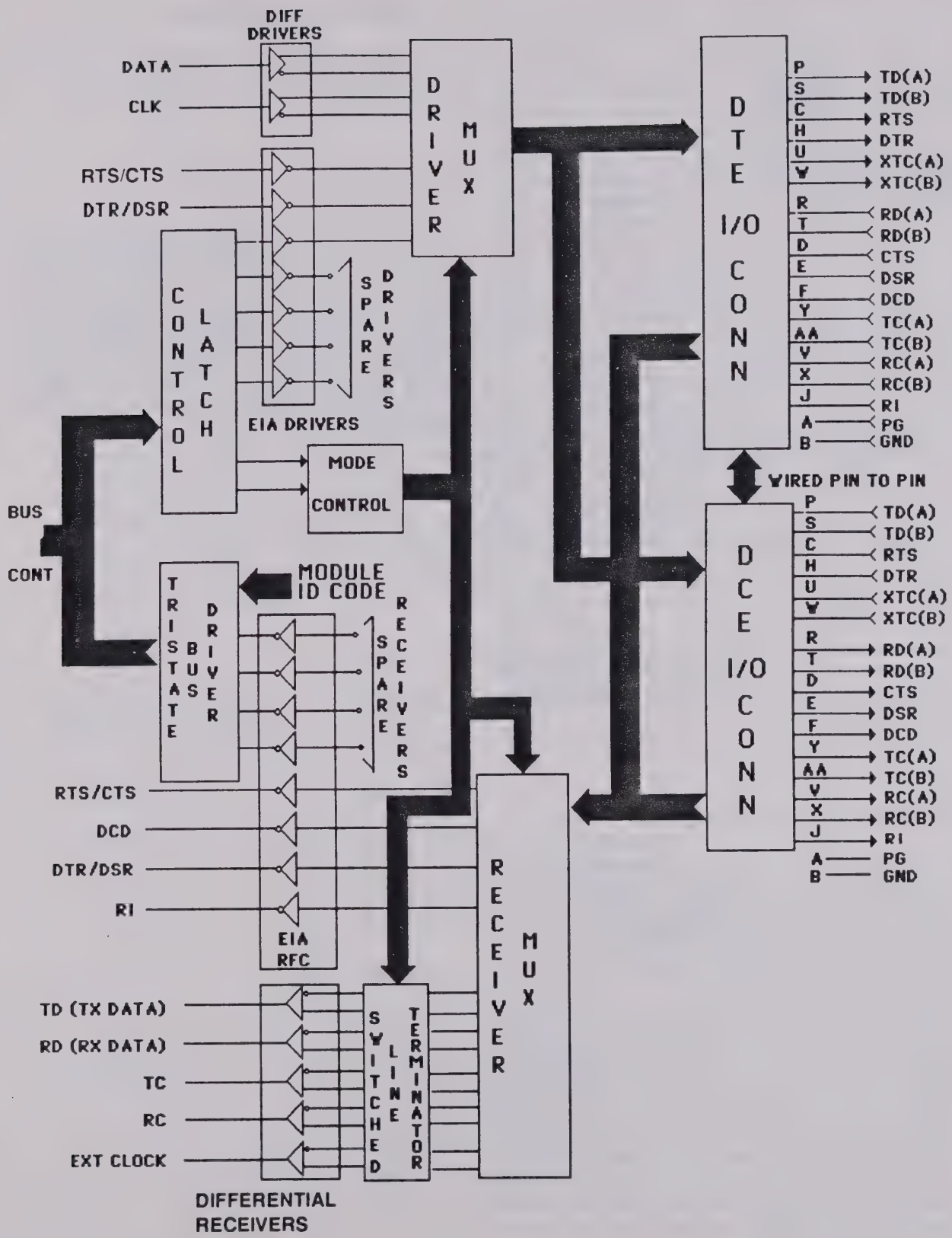


Figure 2-1. Model 5500-300 CCITT V.35 Interface Module Block Diagram

The electrical interface between V.35 equipment and the internal TTL levels is accomplished by the balanced differential drivers and receivers. The signaling information such as RTS, CTS and other DC signals is converted using the EIA RS-232 drivers and receivers in accordance with CCITT recommendation V.28. The Receiver Multiplexer takes signals from DCE and DTE connectors, and feeds them to the appropriate balanced differential, or EIA receiver for conversion to TTL level and processing within the Model 5500 logic. The Receiver Multiplexer also feeds the appropriate received data and clock signals through the switched line terminations before the balanced receivers. The Mode Control logic controls the configuration of the Module for DCE or DTE testing, and selects the appropriate terminating impedance as well as the operation of the Receiver and Driver Multiplexers to generate and receive the correct signals on the DCE or DTE I/O connectors. The Model 5500 logic controls the operation of the interface module through the control bus which interfaces to the module through the TRI-STATE BUS Driver and Control Latch devices. The Module ID code, which informs the Model 5500 that the V.35 module is plugged in, feeds into the Tri-State Bus Driver along with spare EIA receivers for future enhancements. The Control Latch converts the information on the Control Bus to signals to drive the Mode Control logic to simulate DCE or DTE Modes of operation. The balanced differential drivers and EIA drivers are fed to the appropriate pins on the DTE and DCE I/O connectors by the Driver Multiplexer which is controlled by the Mode Control logic.

3.0 OPERATION

3.1 DTE CONFIGURATION

The DTE Mode is selected by toggling the DCE/DTE front panel key to obtain the DTE indication on the CRT display. In the EXTERNAL CLOCK mode, the Model 5500 derives its timing from the DCE under test on the Serial Transmit Clock leads Y and AA or from the USER CLOCK BNC connector.

In turn, the Model 5500 generates Transmit Data and External Transmit Clock on pins P, S, and U, W, respectively. The Model 5500 detects Receive Data on pins R, T, and receive Clock on pins V and X. If the user selects an internal bit rate the Model 5500 becomes the clock source for the test set up. The unit generates transmit data, and clock on pins R, S and U, W, respectively. The internal bit rate of the Model 5500 may be set to any value between 50 bps, and 13 Mbps using the USER CLOCK rear panel BNC jack input to apply an external clock source.

3.1.1 Controls and Indicators

RTS and DTR states are controlled by the front panel keys. DSR, DCD, CTS, RD, TD, RC, TC, and XTC states are also displayed on the front panel LED's.

3.2 DCE CONFIGURATION

When configured as a DCE the Model 5500 generates and supplies clock to the DTE on pins BB and Z (Serial Clock Transmit). The DTE returns Send Data on pins P and S to the Model 5500 in sync with the Serial Clock Transmit on pins BB and Z. The Model 5500 also generates Serial Clock Receive (SCR), and Receive Data (RD) on pins V, X and R, I, respectively and transmits them to the DTE under test. DCD and DSR can be toggled from the front panel keys and all primary leads status indicated on the LED's.

Model 5500-450

RS-449/MIL-188-114 Interface Module

1.0 INTRODUCTION

The Model 5500-450 RS-449/MIL-188-114 Interface Module option is designed to provide the balanced (RS-422) and unbalanced (RS-423) electrical interfaces of RS-449 and MIL-188-114. The electrical interface parameters of MIL- STD-188-114 are intentionally and directly equivalent to RS-449 parameters with the exception of the balanced generator offset voltage which is restricted to a value of ±0.4 volts max for MIL-STD-188-114 (RS-449 allows ±3.0 volts max). The model 5500-450 Interface module balanced generators are balanced to ground with offset voltage less than ±0.4 volt; therefore, this module is completely compatible with both MIL-STD-188-114 and RS- 449. EIA RS-449 defines two categories of interchange circuits; Category I and II. Category I circuits with data rates of 20 Kbps or less may use either the balanced or unbalanced electrical characteristics. Above 20 Kbps all Category I circuits should use the RS-422 balanced characteristics. Category II circuits can use the unbalanced RS-423 electrical characteristics. Examples of Category II circuits are: Select frequency (SF), Signaling Rate Selector (SR), and Signaling Rate Indicator (SI).

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-450 Interface Module specifications.

Table 2-1. Model 5500-450 Specifications

CHARACTERISTIC	SPECIFICATION
Mode	Synchronous
Emulation	DCE or DTE
Data Rates	DC to 20 Kbps (RS-423 Unbalanced) DC to 13.0 Mbps (RS-422 Balanced)
RS-422 Drivers	Impedance: <100 ohms Differential Output Voltage between 2 Volts and 6 Volts
	Short Circuit Current: less than 150 ma.
	Output rise Time less than 20 nsec.
RS-422 Receivers	Impedance: 100 ohms terminated >1K ohms un-terminated.
	Differential Input Voltage
	Threshold: > ±0.2 volts

Table 2-1. Model 5500-450 Specifications (Cont)

CHARACTERISTIC	SPECIFICATION
RS-423 Drivers	Open Circuit Voltage Magnitude between 4 and 6 volts.
	Source Impedance: 50 ohms nominal.
	Output Voltage Magnitude: 3.6 to 5.4 volts with 450 ohm load.
	Short Circuit Current: < 150 ma.
RS-423 Receivers	Impedance: 450 ohms terminated. >1K ohms unterminated
	Differential Input Voltage: > ±0.2 volts
Data Mark (Binary 1 or or OFF State)	A terminal more negative than B - RS-422 (Balanced)
	A terminal Negative Polarity RS-423 (Unbalanced)
Data Space (Binary 0 or On State):	A terminal more positive than B - RS-422 (Balanced)
	A terminal Positive Polarity RS-423 (Unbalanced)

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-450 RS-449/MIL-188-114 interface module option is designed to permit the Model 5500 to be configured as a DCE or DTE device and to test both RS-422 and RS-423 (and equivalent MIL-188-114) electrical characteristics. The RS-449/MIL-188-114 standards cover the exchange of synchronous, serial format data in both balanced (RS-422) and unbalanced (RS-423) modes at data rates up to 2.0 Mbps. (The 5500-450 will operate at data rates up to 13.0 Mbps.)

A block diagram of the RS-449/MIL-188-114 Interface Module is shown in figure 2-1. The mechanical interface is provided by two 37 pin I/O connectors; DTE female and DCE male. Table 2-2 presents the RS-449 connector pin assignments.

Signals into the Model 5500 are fed from the DTE and DCE connector pins to the Line Terminator Switch and differential receivers for conversion to TTL levels and analysis by the Model 5500. The operation of the module is controlled over the Control Bus which interfaces the Model 5500 to the Control Latch and Bus Driver circuits on the Module. The mode control logic on the interface Module enables the appropriate tri-state Receivers and Drivers to set the configuration of the units as DCE or DTE.

3.3 OPERATION

Selection of Balanced (RS-422) or Unbalanced (RS-423) drivers is accomplished by activating an alternate action push button switch on the module rear connector panel. Likewise, selection of Terminated or Unterminated receivers is also made with a push button switch. Four LED's indicate the selected mode of operation. When operating in the Terminated mode, the Balanced/Unbalanced switch automatically selects the appropriate termination resistance for each receiver (100 ohms for balanced, 450 ohms for unbalanced).

Table 2-2. RS-449 Interface Connector Pin Assignments

FIRST SEGMENT ASSIGNMENT			SECOND SEGMENT ASSIGNMENT			CIRCUIT CATEGORY	DIRECTION	
CONTACT NUMBER	CIRCUIT	INTERCHANGE POINTS*	CONTACT NUMBER	CIRCUIT	INTERCHANGE POINTS*		TO DCE	FROM DCE
1	SHIELD	--						
2	SI	A-A'	20	RC	C-B'	II		X
3	SPARE		21	SPARE				
4	SD	A-A'	22	SD	B/C-B'	I	X	
5	ST	A-A'	23	ST	B/C-B'	I		X
6	RD	A-A'	24	RD	B/C-B'	I		X
7	RS	A-A'	25	RS	B/C-B'	I	X	
8	RT	A-A'	26	RT	B/C-B'	I		X
9	CS	A-A'	27	CS	B/C-B'	I		X
10	LL	A-A'	28	IS	A-A'	II	X	
11	DM	A-A'	29	DM	B/C-B'	I		X
12	TR	A-A'	30	TR	B/C-B'	I	X	
13	RR	A-A'	31	RR	B/C-B'	I		X
14	RL	A-A'	32	SS	A-A'	II	X	
15	IC	A-A'	33	SQ	A-A'	II		X
16	SF/SR+	A-A'	34	NS	A-A'	II	X	
17	TT	A-A'	35	TT	B/C-B'	I	X	
18	TM	A-A'	36	SB	A-A'	II		X
19	SG	C-C'	37	SC	C-B'	I	X	

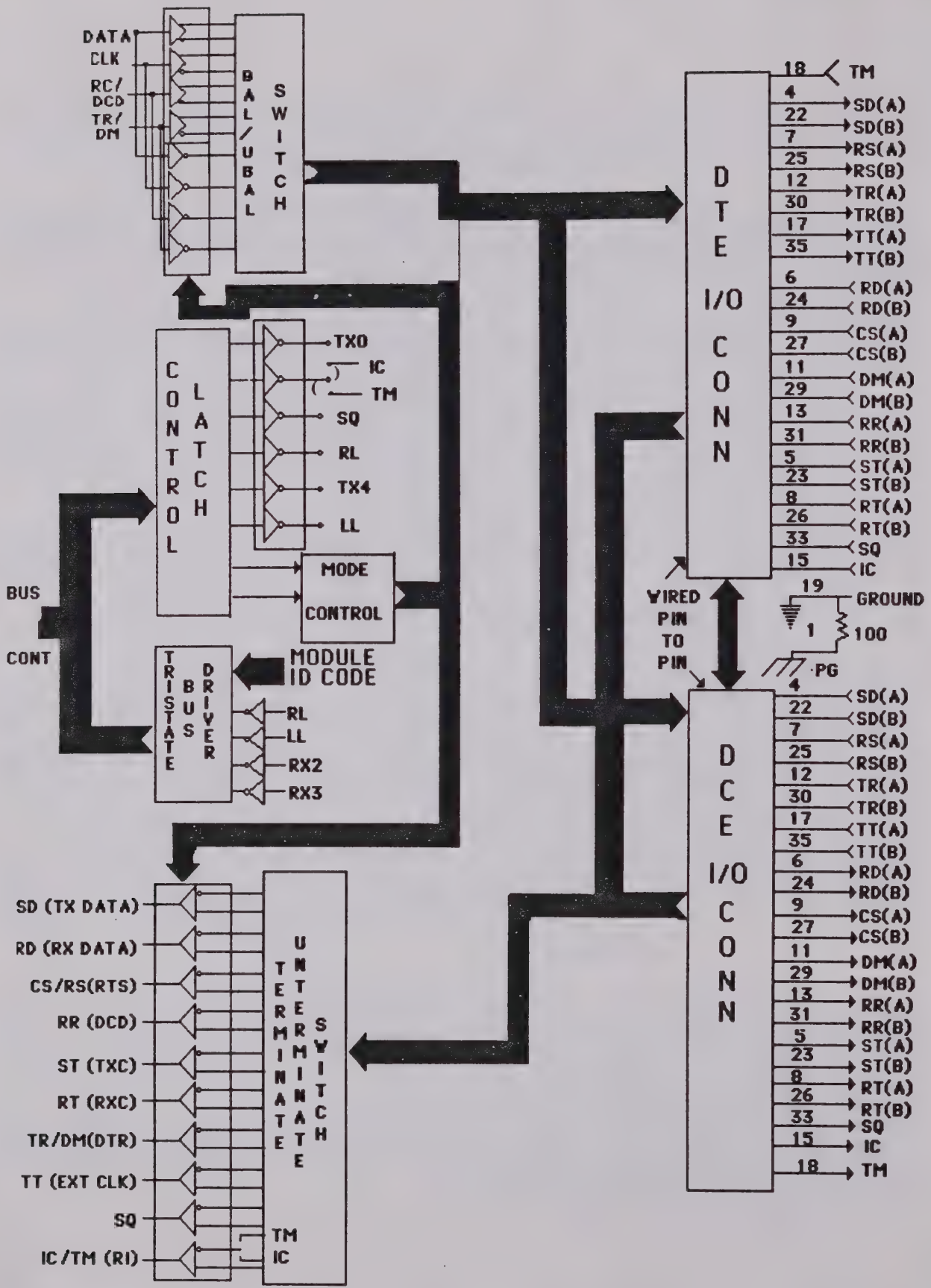


Figure 2-1. RS-449/MIL-188-114 Block Diagram

3.1 REMOTE CONTROL

The Model 450 RS-449 module includes provisions for activating and/or monitoring the status of several special function RS-449 control lines. Because there are no front panel switches to control or indicate status of these functions, the control/monitor capability is provided via the remote control port (RS-232 or IEEE-488) of the Model 5500. The supported functions include Local Loopback, Remote Loopback, Ring Indicator, Test Mode, Signal Quality, 2 spare differential drivers, and one spare TTL receiver (for remote monitoring of any of the TTL level signals on the interface module). Figure 3-2 shows PC board layout for pads referenced in table 3-1.

Table 3-1. Remote Port Control Functions

Remote Control Designation	Model 450 RS-449
TXØ	Spare balanced differential ± 5 volt driver (DTE or DCE mode). Pads on PC board marked "TXØ-A" and "TXØ-B". TXØ-A inverted output, TXØ-B non-inverted output.
TX1	"RI" or "TM" driver (DCE mode). Jumper selectable to "RI" or "TM" on PC board (shipped "RI").
TX2	"SQ" driver (DCE mode).
TX3	"RL" driver (DTE mode).
TX4	Spare balanced differential ±5 volt driver (DTE or DCE mode). Pads on PC board marked "TX4-A" and "TX4-B". TX4-A inverted output, TX4-B non-inverted output.
TX5	"LL" driver (DTE mode).
RXØ	"RL" receiver (DTE or DCE mode).
RX1	"LL" receiver (DTE or DCE mode).
RX2	Spare TTL receiver (DTE or DCE mode). Pad on PC board marked "RX2". May be hard wire jumpered to any TTL signal on the board for sampling via the remote port.
RX3	"SQ" receiver (DTE or DCE mode). Note 1: Resistor R155 (10 ohms) may be removed and RX3 may then be used as a second spare TTL receiver. Pin 8 of U12 is the connect point for the RX3 TTL level test points. Note 2: "SQ" status is indicated by a front panel LED in addition to accessibility via the remote port as RX3. Note 3: "RI/TM" status is indicated by the front panel LED labeled "RI". A jumper on the PC board may be positioned to monitor either "RI' or "TM". (The "RI/TM" status is not accessible via the remote port.)

3.2 TTL TEST SIGNALS

TTL test signals, presented in table 3-2, may be found at the following nodes in the event they are to be jumpered to either the "RX2" TTL receiver or the "RX3" TTL receiver (if R155 is removed).

Table 3-2. TTL Test Signals

TTL Test Signal Node	DTE Function	DCE Function
U13-3	SD	SD
U9-13	RD	SD
U10-13	ST	ST
U10-11	RT	RT
U13-13	TT	TT
U9-11	DM	TR
U9-5	CS	RS
U9-3	RR	CS

Note: **Bold** indicates an inverted line.

3.3 REMOTE COMMANDS

The remote port command for TX drivers is as follows:

> TXØ T "Return" (Sets TXØ to logic true)
> TXØ F "Return" (Sets TXØ to logic false)

To determine the current state of a driver, the command is:

> TXØ "Return" (Asks the status of the TXØ driver)
> FALSE (Command response indicates requested status).

To determine the current state of a receiver, the command is:

> RXØ "Return" (Asks status of RXØ receiver).

> TRUE (Command response indicates requested status).

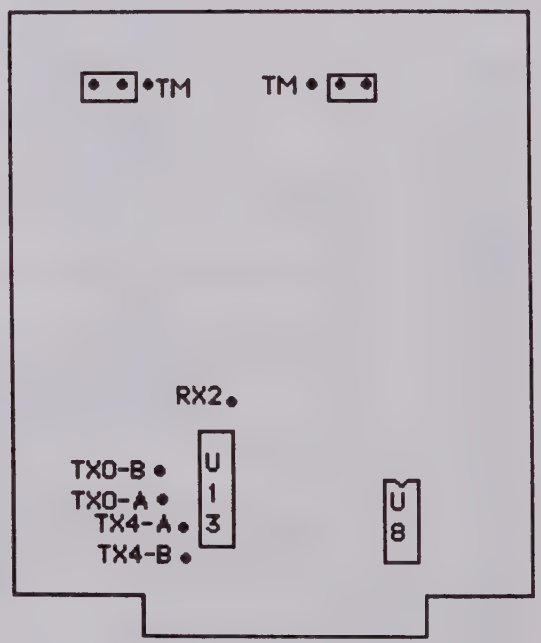


Figure 3-2. PC Board Layout

Model 5500-500

TTL Interface Module

1.0 INTRODUCTION

The Model 5500-500 TTL Interface Module has the same physical connectors and pin assignments as the standard EIA RS-232 25 pin interface; however, the logic is inverted on all data, clock and control lines (relative to standard EIA RS-232 logic convention). DCE or DTE emulation and SYNC or ASYNC mode operation are controlled and switchable from the Model 5500 front panel keys or by commands over the remote ports. The function and operation of this module is identical to that of the Model 5500-200 RS-232 Interface Module, except for the use of TTL gates and logic inversion on all I/O lines.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-500 TTL Interface Module specifications.

Table 2-1. Model 5500-500 Specifications

CHARACTERISTIC	SPECIFICATION
Modes	Synchronous or Asynchronous
Date Rates	50 bps to 48.0 kbps Asynchronous 50 bps to 4.0 mbps Synchronous
Character Size	5, 6, 7, or 8 data bits
Parity	Odd, Even, or No parity bits
Stop Bits	1 or 2 bits
Input Data Characteristics	MARK signal, binary state 1, or OFF = TTL logic 1.
	SPACE signal, binary state O, or ON = TTL logic O.
Line Drivers	CLK & DATA = "74128" 75 - ohm Drivers
	Control & Status "7408" GATES
Line Receiver	"74HCTO8" GATES

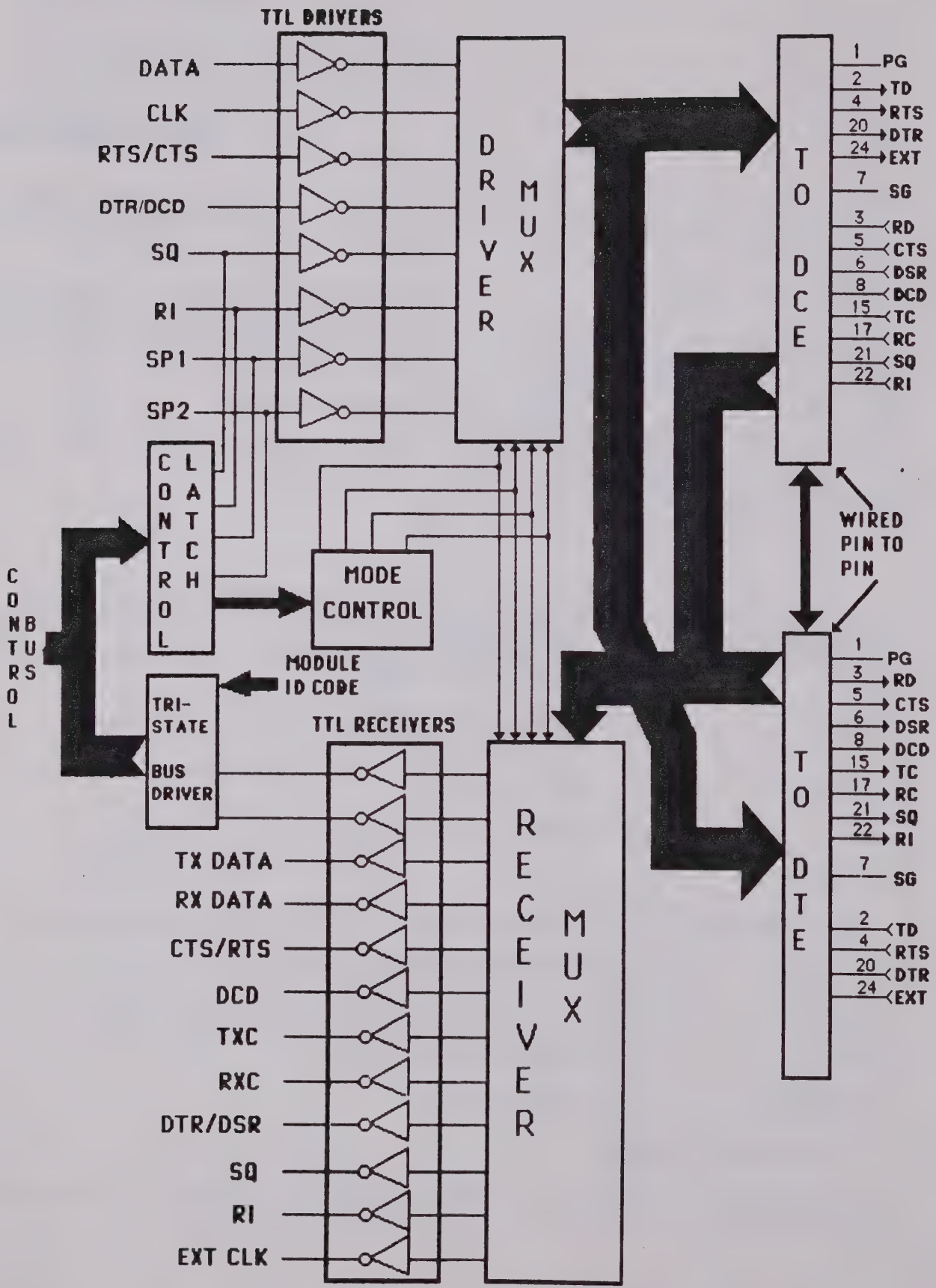


Figure 2-1 TTL Interface Block Diagram

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-500 TTL interface is capable of operation in Synchronous and Asynchronous modes with both DCE and DTE configurations. The module has two 25 pin subminiature 'D' type connectors, Male for DCE and Female for DTE. In addition, the DCE/DTE emulation is electronically switchable from the Model 5500 front panel or via commands over either remote control port. Figure 2-1 presents a simplified block diagram of the Model 5500-200 module.

3.0 OPERATION

3.1 DATA TERMINAL EQUIPMENT (DTE) CONFIGURATION

The Model 5500 may be configured as Data Terminal Equipment (DTE) for testing data Communications Equipment (DCE) such as Modems, Multiplexers, or other peripheral equipments configured as DCE. This is accomplished by toggling the front panel key labeled 'DCE/DTE' until DTE appears in the upper left hand corner of the BERT CRT display (refer to section 3.2 of this instruction book for location and description of the Model 5500 controls and indicators). In the Synchronous mode of operation the Model 5500 may be set to derive clock from the equipment under test or it may generate the clock internally and provide clock to the equipment under test.

In the Asynchronous mode of operation, data is transmitted and received without a clock. Start and stop bits provide proper decoding of the data bits in each character (byte) sent while timing is extracted from the bit transitions. In Synchronous operation, with the DCE under test acting as the source of timing, the Model 5500 bit rate selection should be set to EXTERNAL. In this position the Model 5500 will derive clock from pin 15 (Transmission Signal Element Timing-DCE Source) of the DTE I/O Connector on the interface module. Transmit data and clock are available on pins 2 and 24 respectively, and receive data and clock are available at pins 3 and 17 respectively.

If a Bit Rate is selected on the Model 5500 then the internal generator of the test set supplies the clock signal to the equipment under test. If the user desires to test at a non-standard bit rate the unit can also be operated with an externally applied USER CLOCK into the rear panel BNC connector with the Model 5500 Bit Rate menu set to USER. The frequency of this externally applied clock is read on the CRT display by scrolling through the frequency selections to the appropriate option-either TC or BR.

In either case the test set ignores signals present on pin 15 of the I/O connector; Transmit data and clock are on pins 2 and 24 and Receive data and clock are on pins 3 and 17, respectively.

When operated in an Asynchronous mode the Model 5500 bit rates are internally generated. The appropriate character size, number of stop bits, and parity must also be selected using the front panel cursor and select keys. In this mode of operation no clock signals are transmitted. Transmit data appears on pin 2 and receive data on pin 15 and 17 are ignored. The Model 5500 recovers clock from the received data transitions to provide internal synchronization to the received patterns.

3.2 DATA COMMUNICATION EQUIPMENT (DCE) CONFIGURATION

The Model 5500 may also be configured to operate as a DCE by toggling the DCE/DTE front panel key until the DCE indication appears in the upper left hand corner of the CRT display. Again, either synchronous or asynchronous peripherals can be tested as in the DTE configuration.

In synchronous mode, the Model 5500 may derive clock from the DTE under test or supply clock to the equipment from its own internal generator. When set to CLOCK, the Model 5500 receives timing from the DTE Transmit Signal Element Timing on pin 24 of the rear panel DTE I/O connector. The frequency of the external clock is read on the CRT display by scrolling through the frequency selections to XC. Under this condition the Transmit Data on pin 2 and Transmit Signal Element Timing on pin 24 are analyzed by the Model 5500.

The Model 5500 generates Receive Data on pin 3 and Receive Signal Element Timing on pin 17 in accordance with the DTE supplied clock on pin 24.

To have the Model 5500 supply clock for the equipment under test it is necessary to select the desired bit rate instead of EXTERNAL. In this case, the Model 5500 supplies timing to the DTE under test on pin 15 of the I/O connector. The Model 5500 analyzes the Transmit Data on pin 2 and Transmit Signal Timing on pin 15 Receive Data on pin 3 and Receive Signal Element timing on pin 17 are generated from the Model 5500 internal clock source. A user supplied external clock signal into the USER CLOCK BNC jack will cause the Model 5500 to generate data and clock at the externally applied clock rate when the Model 5500 is set to USER on the BIT RATE menu.

Asynchronous DCE mode operation of the Model 5500 requires selection of the ASYNC mode, bit rate, character size, parity, and number of stop bits. Data is generated and received in character format with no clock signals provided.

Timing is derived from the data transitions and the start and stop bits location identifies the data (character) and parity bits to the receiver for proper decoding.

3.3 CONTROLS AND INDICATORS

Front panel keys labeled RTS/DCD and DTR/DSR enable the user to turn RTS and DTR ON and OFF when the Model 5500 is configured as a DTE.

Twelve green LED's provide visual indication of the primary lead status as follows:

Transmit Data	(TD)
Receive Data	(RD)
Transmit Clock	(TC)
Receive Clock	(RC)
Request to Send	(RTS)
Clear to Send	(CTS)
Data Set Ready	(DSR)
Data Terminal Ready	(DTR)
Data Carrier Detect	(DCD)
Ring Indication	(RI)
Signal Quality	(SQ)
Transmit Clock External	(SCTE).

The front panel key labeled DCE/DTE electronically switches the rear panel I/O Connector functions from DCE to DTE and vice versa. This eliminates the need for special cables to use with the TTL interface module. These and any other functions and indications may be accomplished and displayed at a remote terminal using the RS-232 or IEEE-488 remote control ports. Table 3-3 presents the TTL connector pin assignments.

Table 3-3. TTL Connector Pin Assignments

Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
					From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	AA	101	Protective Ground	X						
2	BA	103	Transmitted Data			X				
3	BB	104	Received Data		X					
4	CA	105	Request to Send					X		
5	CB	106	Clear to Send				X			
6	CC	107	Data Set Ready				X			
7	AB	102	Signal Ground (Common Return)	X						
8	CF	109	Received Line Signal Detector				X			
9			(Reserved for Data Set Testing)							
10			(Reserved for Data Set Testing)							
11			Unassigned							
12	SCF	122	Sec. Rec'd. Line Signal Detector				X			
13	SCB	121	Sec. Clear to Send				X			
14	SBA	118	Secondary Transmitted Data			X				
15	DB	114	Sig. Element Timing (DCE Source)						X	
16	SBB	119	Secondary Received Data		X					
17	DD	115	Rec. Sig. Element Timing (DCE Source)						X	
18			Unassigned							
19	SCA	120	Secondary Request to Send					X		
20	CD	108.2	Data Terminal Ready					X		
21	CG	110	Signal Quality Detector				X			
22	CE	125	Ring Indicator				X			
23	CH/CI	111/112	Data Signal Rate Selector (DTE/DCE Source)				X	X		
24	DA	113	Xmit. Sig. Element Timing (DTE Source)							X
25			Unassigned							

Module Switching Unit System

Model 5500-555 MSU I/O Control Module

Model 5500-MSU Module Switching Unit

1.0 INTRODUCTION

The Module Switching Unit System provides the capability to select up to 16 interface modules for use with the Model 5500. The system is modular and may be expanded to switch from as few as two modules up to the maximum of 16 via Module Switching Units that switch up to 4 modules each. This capability eliminates the need to change plug-in modules from the rear of the Model 5500 and enables the user to configure up to 16 separate data channels for test by the Model 5500. The MSU system is compatible with all Model 5500 interface modules and the modules may be installed in the MSU system in any combination, type or quantity, up to the maximum of 16.

Two modes of operation are provided by the MSU system. The MANUAL mode allows the user to select any one of up to 16 modules for "on line" operation via pushbutton selection on the front panel of the Model 5500-MSU. The AUTO mode allows the user to remotely select the "on-line" module from the front panel of the Model 5500.

The complete MSU system (refer to Figure 1-1) consists of the Model 5500-555 MSU I/O Control Module, and four Model 5500-MSU Module Switching Units. The Model 5500-555 MSU I/O Control Module plugs into the interface module slot in the rear of the Model 5500 and provides the control functions for the Model 5500-MSU Module Switching Units. Each Model 5500-MSU Module Switching Unit contains switching provisions for four interface modules. Up to four Model 5500-MSU's may be controlled by a Model 5500-555 MSU I/O Control Module to provide expandable switching capability for up to 16 interface modules.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-MSU Module Switching Unit.

2.1 FUNCTIONAL DESCRIPTION

The complete MSU system provides the user with the capability to switch up to 16 interface modules for "on line" use by the Model 5500. These 16 interface modules can consist of any combination of module types available for the Model 5500. With the MSU system installed, the user can manually select any of the 16 modules via pushbuttons located on the front panels of the Model 5500-MSU Module Switching Units or by automatic selection via the Model 5500 using either the front panel soft keys and display menu or the remote port on the Model 5500.

The Model 5500-555 MSU I/O Control Module (refer to Figure 2-1) provides all of the command and control functions for up to four Model 5500-MSU's. With the selector switch in the MAN position, the MSU I/O Control Module accepts module selection request commands from the module selector pushbuttons located on the front panel of the MSU's, via connector J2. These switch selections are decoded by the internal control logic and a "Module Enable" command is sent to the corresponding MSU to place the selected module "on line". With the selector switch in the AUTO position, module selection can be performed via the Model 5500 (refer to MSU configuration menu in Section 3) in addition to the pushbuttons on the front panel of the MSU's. When performing module selection via the Model 5500, the user selects the desired module from the MSU configuration menu or via the remote port. The Model 5500, in turn, sends a command to the control logic of the MSU I/O Control Module to place the desired module "on line". The MSU I/O Control Module then sends a "Module Enable" command to the corresponding MSU. When performing module selection via MSU front panel pushbuttons, in the AUTO mode, pushbutton selections are passed to the Model 5500 via the MSU I/O Control Module. The Model 5500 then commands the MSU I/O Control Module to enable the selected module as described above. A remote lockout feature is included in the Model 5500 MSU configuration menu that can be enabled to prohibit module selection via the MSU front panel pushbuttons.

Table 2-1. Model 5500-555 Specifications

CHARACTERISTIC	SPECIFICATION
Dimensions:	17.20" W. x 5.25" EIA (5.22") H x 12.79"D
Weight:	18 lbs. (approx.) excluding modules
Power:	Selectable 115/230 VAC ± 12% 47 to 60 Hz. 26W standby, 40W on line (max)
Environmental:	0 to 50 degrees C (operating) -10 to 85 degrees C (storage)
Front Panel Controls, and Indicators:	Module select momentary pushbutton, Module "ON LINE" LED indicators, Chassis 'ON LINE" LED indicators, Chassis ID CODE selection switch, Power ON/OFF LED indicator.
Rear Panel Controls, and signal access:	Power ON/OFF switch controls operation in conjunction with Model 5500. 2-Dual 50 pin ribbon cable jack pairs for daisy-chain configuration.

Once a module has been placed "on line", the MSU system becomes transparent to both the "on line" module and the Model 5500. This transparency remains in effect until a new module is selected. The MSU I/O Control Module as well as the Model 5500-MSU Module Switching Unit contain differential line drivers and receivers to pass all of the Model 5500 module interface signals between the Model 5500 and the "on line" module.

The Model 5500-MSU Module Switching Unit (refer to Figure 2-2) provides the switching capability for four interface modules. Up to four MSU's may be controlled from a single MSU I/O Control Module. Each MSU must be assigned a sequential chassis ID code via the chassis ID code switch on the front panel upon installation. If two MSU's are utilized they must be assigned chassis ID codes 1 and 2 respectively, if four MSU's are utilized, they must be assigned chassis ID codes 1, 2, 3 and 4 and so on. This chassis ID code provides identification of each MSU to be utilized during command sequences. When a "Module Enable" command is sent by the MSU I/O Control Module, each MSU decodes a portion of the command to extract the chassis ID code. If the chassis ID code matches the switch setting, the MSU decodes the remainder of the "Module Enable" command to place the desired module "on line". This is accomplished by enabling corresponding tri-state buffers, a power relay, and an indicator LED to signify which module is "on line". A chassis "ON LINE" LED is illuminated whenever one of the modules in an MSU is "on line".

Expansion of the MSU system (refer to Figure 2-3) from one to four MSU's is accomplished by connecting the MSU's together in a daisy-chain fashion. Terminating adapters, supplied with the Model 5500-555 MSU I/O Control Module must be installed on the last MSU in the chain. The J1A&B connectors are keyed differently than the J2A&B connectors, as are the supplied cables, to prevent interconnection mistakes.

Power to the MSU is controlled via the on/off switch on the rear panel of the MSU in conjunction with the Model 5500. Both the Model 5500 power switch and the MSU power switch must be on to enable power to the MSU system.

The MSU can be configured to operate on either 110 VAC or 230 VAC by removing the top cover and selecting the line voltage via the selector switch on the AC input module.

Modules may be inserted or removed from the MSU with power on, since power is not applied to a module slot until the module is selected. However, the user should take precautions no to insert or remove a module when the module slot is selected, otherwise damage may occur to the module or to the MSU.

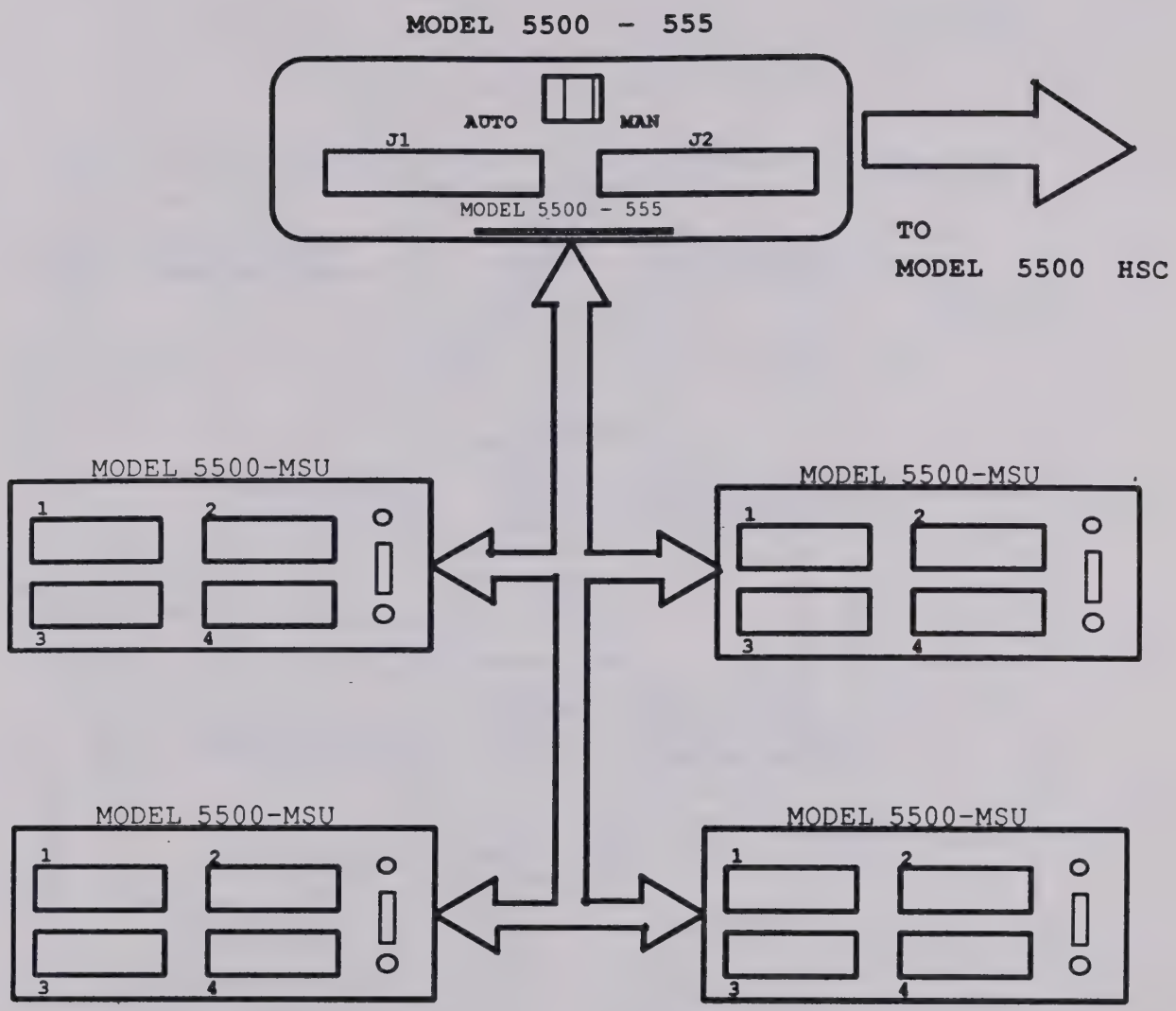


Figure 1-1. MSU System Block Diagram

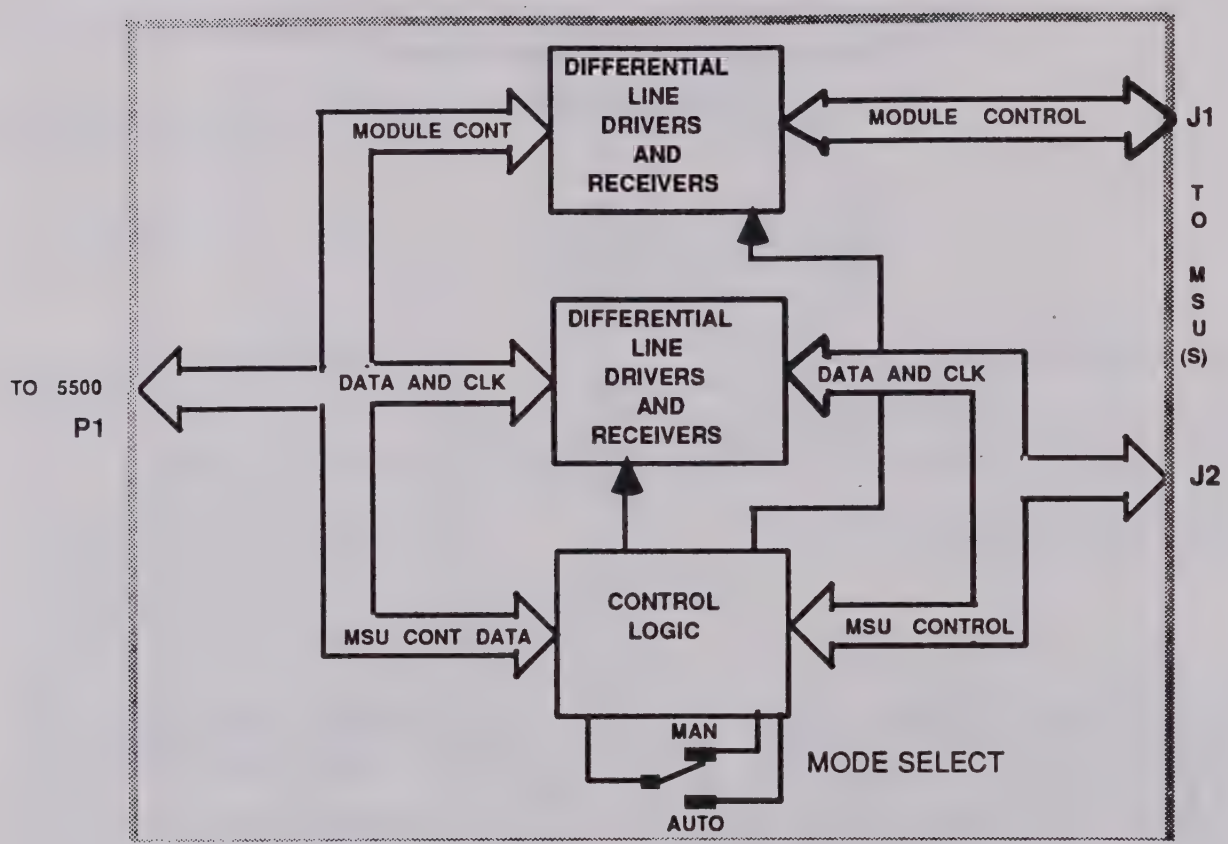


Figure 2-1. Model 5500-555 MSU I/O Control Module Block Diagram

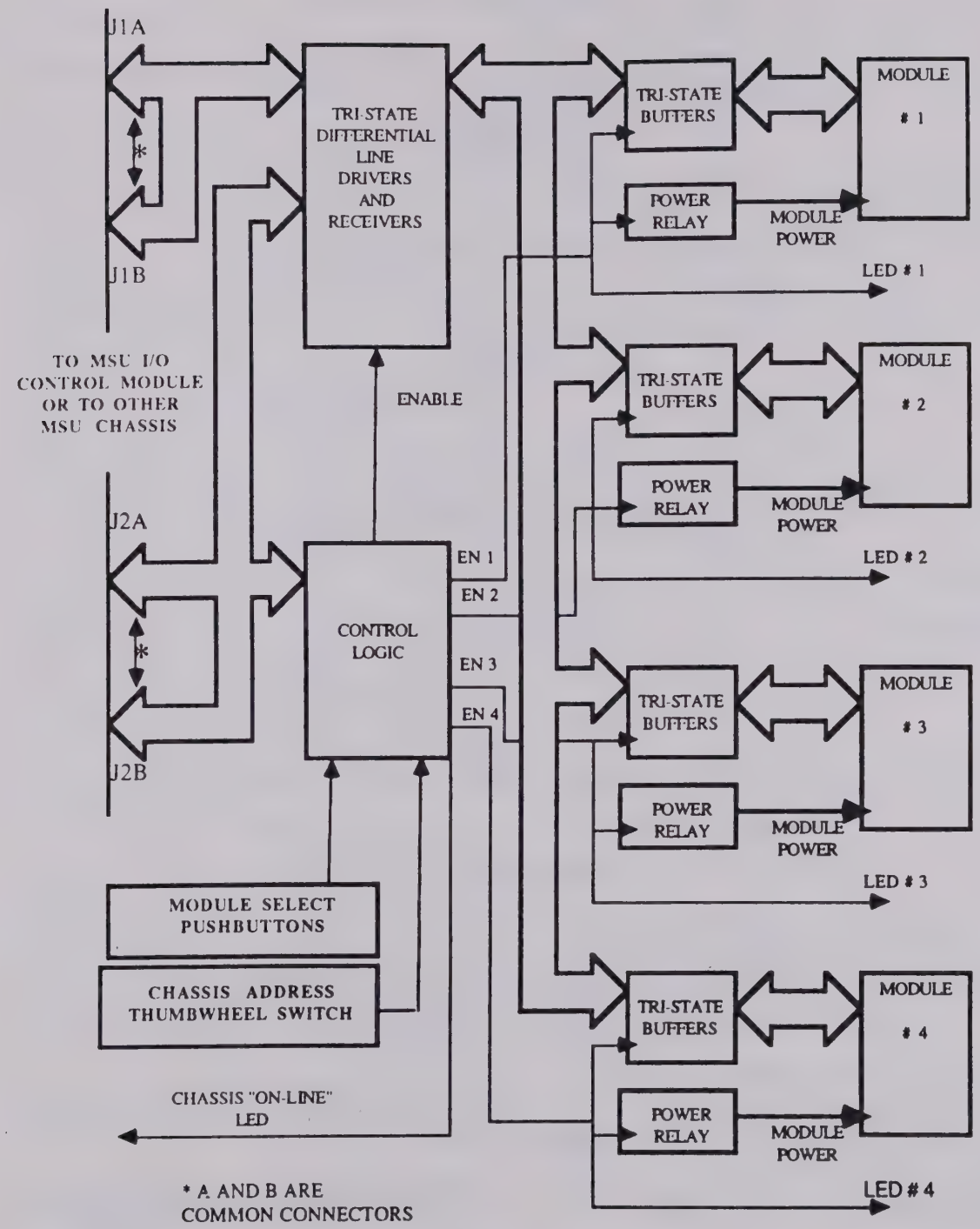


Figure 2-2. Model 5500-MSU Module Switching Unit Block Diagram

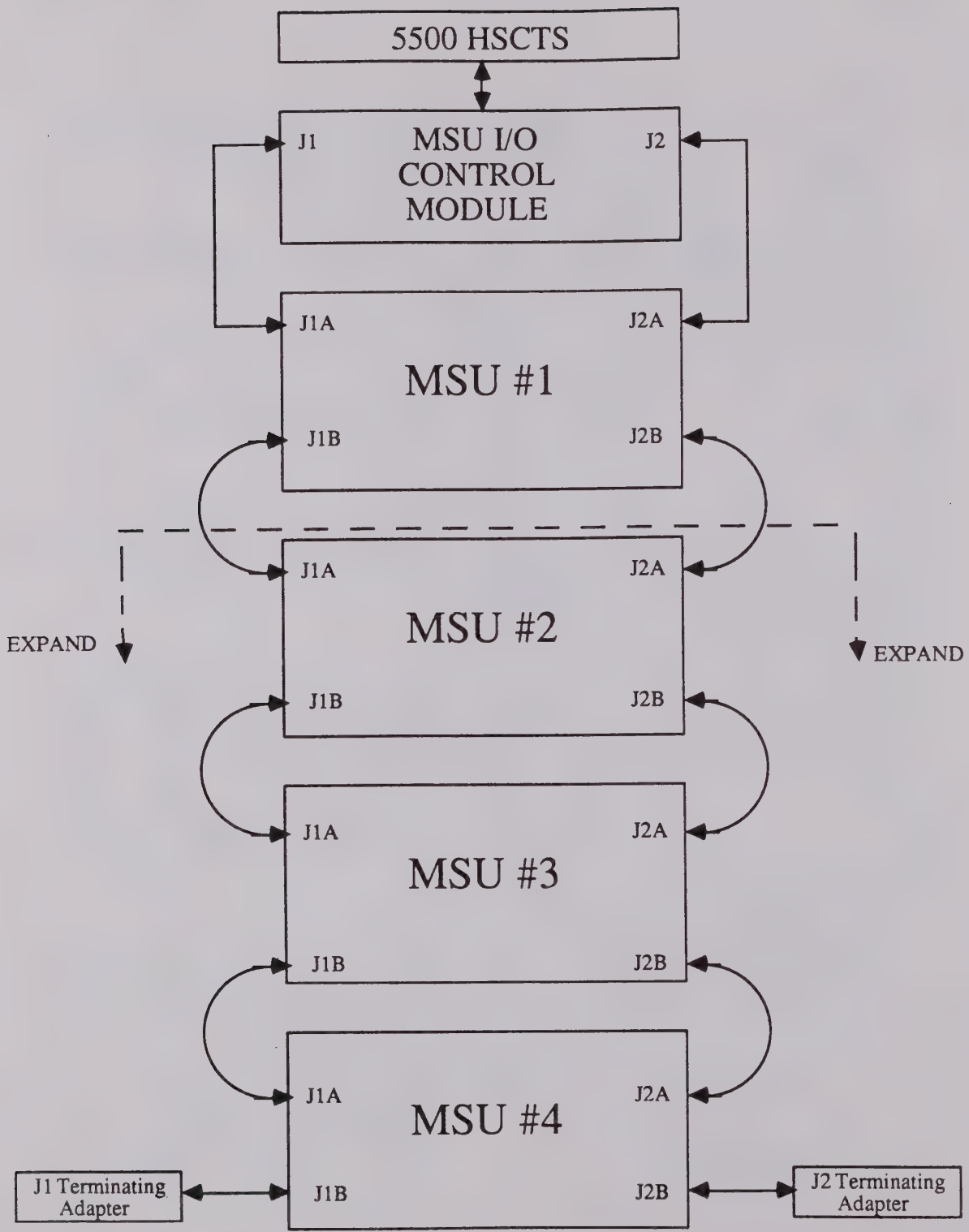


Figure 2-3. MSU System Expansion

3.0 OPERATION

3.1 MSU CONFIGURATION MENU

The MSU Configuration Menu (refer to Figure 3-1) allows the user to control and observe the status of the MSU system via the Model 5500. To select a module, the user moves the cursor to the desired module via the cursor control soft keys and presses either of the two cursor select keys. An asterisk is displayed beside the module to indicate it is "on line" and the module type is displayed at the bottom of the menu. When selecting a module from the MSU front panel pushbuttons, the asterisk will move to indicate the "on line" module as it is selected. The remote lockout feature is enabled or disabled by pressing the adjacent soft keys on the Model 5500 front panel. When a module is selected, a stored operational program must be recalled from the Model 5500 memory (refer to Model 5500 Instruction Book, Section 3 & 4) or the module mode control menus must be reconfigured to place the selected module in the desired mode of operation. Stored programs may also be preassigned to any module slot. To preassign a stored program, the user must position the cursor, via the cursor control soft keys, under the program number column labled "P" and adjacent to the desired module slot. The stored program number may then be assigned by using the hex keypad on the front panel of the Model 5500 or by using the cursor select soft keys. Stored program numbers 0-9 may be assigned directly from the hex keypad or by incrementing or decrementing the program number via the cursor select keys.

Once power is turned on, the Model 5500 interrogates the MSU system to determine module configuration and displays the current MSU configuration on the MSU configuration menu. If a module slot is empty, "empty" will be displayed next to the module slot identification characters. If all four module slots in an MSU are empty, or if the MSU is not installed, "empty" will be displayed next to all four module slot identification characters.

The Model 5500 will then place a module "on line" corresponding to the last module slot "on line" before power off.

3.2 MSU REMOTE PORT OPERATION

Being consistent with other remote port commands, the MSU remote port operation is intended to provide the user with the capability to accomplish any and all of the same functions provided on the MSU menu as well as provide as much helpful information as possible. To accomplish this two remote port commands are used :

INTERFACE and RLOCK

The interface command is not new, but has been modified to include additional information now needed with the MSU system. Both commands if entered as shown above will return the present setting of the respective functions. The interface command will return a line similar to that shown in Figure 3-2, A.

This informs the user that an MSU system is installed, that the card in chassis #1, slot #2 is presently on line, that the card type is and RS-232, and that the program to be recalled upon the selection of this card is program #4.

To obtain a list of the cards presently installed in the MSU system chassis', a query is added to the command :

INTERFACE ?

This returns a list as presented in Figure 3-2, B.

From this list the user may determine which interface he desires to be on line. To change the on line interface enter the command:

INTERFACE xx where xx = chassis#/slot #

For example, to select chassis #1, slot #3 the user would enter the command :

INTERFACE 13

The optional recalled program number associated with each chassis/slot may also be altered. To reassign chassis #1, slot #1 to program #9, enter:

INTERFACE 11 PROGRAM 9

This will alter only the assigned program number and will not affect the on line module. A blank program number indicates that no program is assigned to recalled for that module, leaving off the "9" in the above command would place a blank in the program number space.

The **RLOCK** command was added to the list of remote port commands to allow access to the status of the MSU system remote lockout. The remote lockout disables the effect of the chassis/slot manual pushbuttons when enabled. To determine the present state of the remote lockout, enter:

RLOCK

This will return the state of the remote lockout as either **DISABLED** (manual switches functional) or **ENABLED** (manual switches non-functional). To effect a change in the status the user would follow the RLOCK command with either **ENABLE** or **DISABLE**:

RLOCK ENABLE

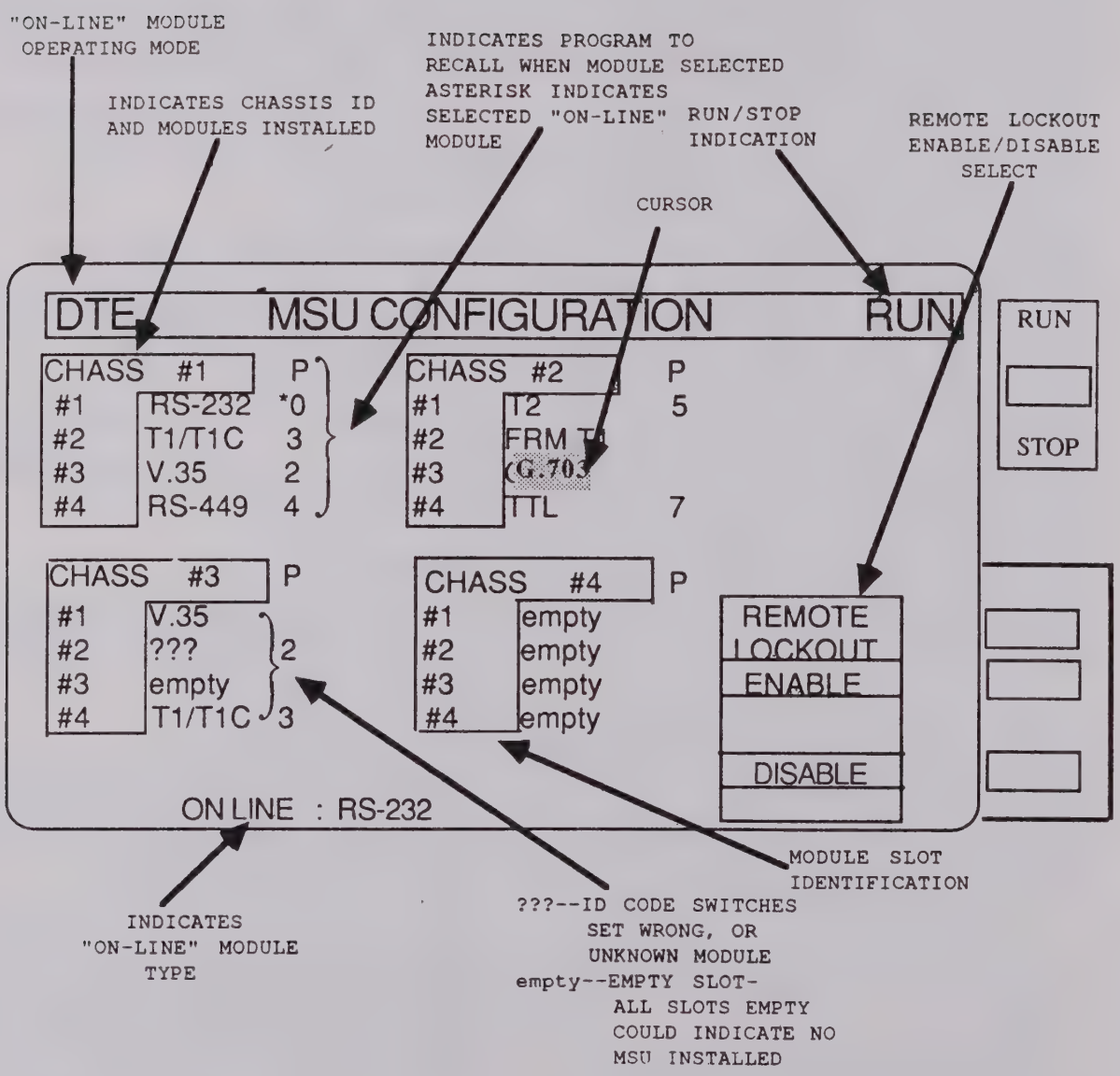


Figure 3-1. MSU Configuration MENU

```
MSU   ( chassis #1 , slot #2 )   CAR   D TYPE : RS-232 ,   PROGRAM 4
```

A

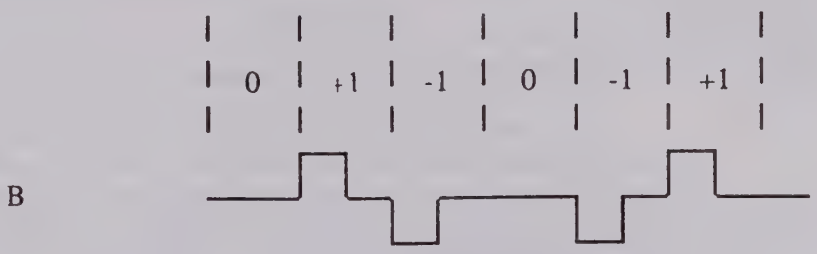
```
MSU   ( chassis #1 , slot #1 )   CAR   D TYPE : V.35    ,   PROGRAM 1
MSU   ( chassis #1 , slot #2 )   CAR   D TYPE : RS-232  ,   PROGRAM 4
MSU   ( chassis #1 , slot #3 )   CAR   D TYPE : T1/T1C  ,   PROGRAM 0
MSU   ( chassis #1 , slot #4 )   CAR   D TYPE : RS-449  ,   PROGRAM 3
MSU   ( chassis #2 , slot #1 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #2 , slot #2 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #2 , slot #3 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #2 , slot #4 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #1 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #2 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #3 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #4 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #1 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #2 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #3 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #4 )   CAR   D TYPE : empty   ,   PROGRAM
```

B

Figure 3-2. Remote Port Responses

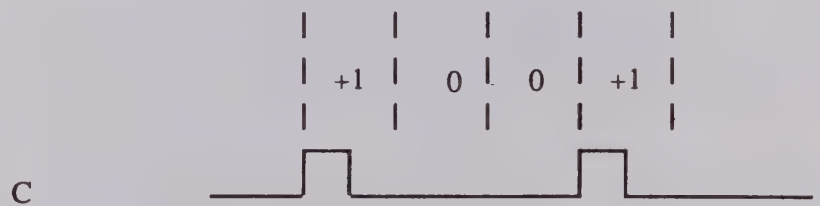
Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION

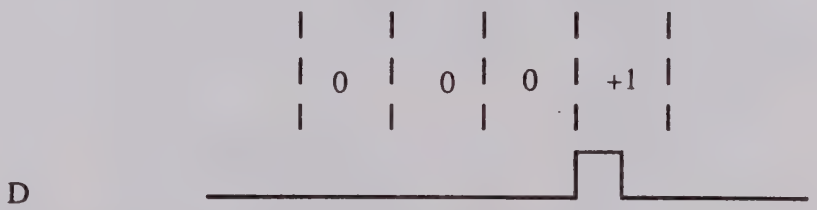


B

Finally, High Density, Bipolar 3 Zero Substitution (HDB3) line coding is used in European T-Carrier systems at 2.048 MBPS and 8.448 MBPS line rates. An example of this coding format is shown if figures C and D. (Preceding violation was negative and preceding pulse was negative in figure C and the preceding violation was negative and the preceding pulse was positve in figure D.)



C



D

The HDB3 coding process generates positive and negative marks alternately each time a binary logical 1 condition occurs within the message signal. However, unlike AMI coding, the maximum number of consecutive zeros is limited to a value of 3. If a series of 4 consecutive zeros does occur, the 4th zero is replaced by a mark referred to as a VIOLATION. The violation mark is always inserted with the same polarity as the preceding mark. This identifies the departure from the AMI scheme and indicates the occurrence of the violation.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
	In theory, if additional safeguards were not taken, it would be possible for several violations to have an identical polarity, and thus introduce a DC component into the signal. To overcome this problem, the coder continuously monitors the polarity of the last violation (may have been many bits earlier in the data stream) and the polarity of the last mark. The coder then forces the first bit of the 4-bit substitution sequence to a one or a zero, whichever is required, to allow the violation in the fourth bit position to be of opposite polarity to the previous violation.
PATTERN	The pattern choices from the regular FORMAT are all present in T-Carrier FORMAT, but the most useful patterns for T-Carrier testing are:
QRW QUASI-RANDOM WORD	A pattern of (2^20)-1 bits long which has built-in suppression of strings of 0's greater than 14. This pattern is the industry standard for T1 and T1C testing. (2^15)-1: A pseudo-random sequence used in European CCITT G.703 BER testing and jitter testing. (2^20)-1: A pseudo-random sequence of the same length as the QRW, but without the 14 zero suppression. Useful at T2 and for CCITT testing.
MARK	An all 1's pattern which may be used to simulate the "idle" pattern sent out by digital channel banks in an alarm condition.
USER	This is a user definable pattern of up to 135 characters (1080 bits) which could be used to send out patterns with more than 14 zeros or any other pattern a user may want to transmit.
T1 SET	This pattern sends out the standard T1 Channel Service Unit (CSU) loopback code (10000) to cause a remote CSU to loopback for test purposes. This code should be transmitted for 5 seconds before the CSU will loopback to prevent false loopbacks.
T1 RESET	This pattern sends out the standard T1 CSU reset code to return a CSU in loopback to normal operation. The code (100) should be sent out for 5 seconds to reset CSU loopback.
BPV INJ RATE	The user may select any rate of injection of Bipolar Violations from 2x10-3 to $1x10^{-7}$ violation/bit. The rate is selected by changing the mantissa from 0 to 9 (a 0 disables the inject function) first and then moving the half intensity block to the right and changing the exponent from -3 to -7 as desired. The select keys or the HEX keypad can be used. A common rate is 1x10-3 which is useful in checking automatic protection switches. Pressing the INJ soft key on the main BERT display activates BPV Injection unless there is a "0" in the BPV inject rate mantissa.
LOGIC ERR RATE	Logic errors are what telephone companies call bit errors to distinguish them from BPV's. This rate of bit error injection is selectable from 9x10-3 to 1x10-9 errors/bit. The errors (and bipolar violations) are uniformly spaced throughout the bit stream when the INJ soft key is pressed. Note that the user is free to have either logic errors or BPV's or both injected.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
CLOCK SOURCE	The user may select from three alternatives depending upon what simulation is being attempted. When the Model 5500 is acting as the generator of the T- Carrier it is normal to choose INTERNAL timing so that the Model 5500 is the master clock. This would be the case whenever any loopback testing is performed. The "RX" or Receive Clock choice allows the user to operate a 5500 in what is called a loop timed mode. That is, the Model 5500 derives clock from the received bit stream and uses this to time its transmitter. This is useful if, for example, the user is making an end to end bit error test with Model 5500's at each end. In this case one of the test sets should be on INTERNAL (acting as the master clock) and the other should be set to RX. The final option available is USER which allows the operator to supply a TTL clock to the rear panel BNC connector. The clock supplied must be at the nominal bit rate of the module being used (i.e. 1.544 MHZ for T1 module, 6.312 MHZ for T2, etc..), and should be at least ±30ppm accurate.

Table 3-2. BER Test Assistance

SYMPTOM	POSSIBLE CAUSE
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Verify that BRIDGE mode in T- Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units.
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when test set stops. This is normal operation.
Model 5500 display errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. NOTE: T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.

Model 5500-624

DS1 (T1) Interface Module

1.0 INTRODUCTION

The Model 5500-624 DS1 (T1) Interface Module enables the Model 5500 to test all types of T-1 Carrier equipments with D4 Superframe Format Framed patterns or Unframed patterns. This feature permits the user to test digital switches, digital access and cross-connect systems, and other devices requiring a framed pattern for test purposes, as well as repeatered lines, multiplexers, channel banks, and Channel Service Units with unframed pattern requirements. The line format is selectable for either AMI or B8ZS. The module functions for signals at normal transmit and receive levels, as well as monitor level signals at the DSX points.

The Model 5500-624 also accepts the Model 5500-J02 Jitter Measurement and Injection Option. The J02 option hardware consists of a PC board which plugs into a special connector on the Model 5500-624 PC board.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-624 DS1 (T1) Interface Module.

Table 2-1. Model 5500-624 Specifications

CHARACTERISTIC	SPECIFICATION
Pulse Rate	1.544 Mbps ±50 ppm Max.
Output Pulse Amplitude	±3.0 V ±10% Into 100 ohms
Output Pulse Width	324 ±30 nsec at 50 percent amplitude
Rise and Fall Times	50 nsec ±25 nsec (10-90%)
Overshoot	Less than 10% of amplitude height.
Reveiver Input	0.5V TO 6.0V peak, ALBO (Automatic Line Build Out) allows operation with up to 4000 feet of PIC22 cable between unit and source.
Input Impedance	100 ohms ±5% terminated. Greater than 1K ohms bridged.

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-624 Framed/Unframed Interface Module enables the Model 5500 to generate and receive T1 serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consists of miniature (bantam) jacks for Transmit, Receive, and a 15 pin subminiature D type connector wired in parallel with the TX and RX bantam jacks.

The Generator section (see figure 2-1) consists of a TX clock select MUX, TX framing logic, a line encoder for AMI or B8ZS, and a bipolar line driver. The Receiver has a switchable line termination of 100 ohms which is disconnected for the high impedance BRDG (Bridge) mode. The receiver section includes an ALBO (Automatic Line Build Out circuit), and Clock Recovery/Data Detector which provide recovered clock and data to the line decoder and RX Frame Sync Logic.

The Line Decoder is set to AMI or B8ZS as appropriate and converts the line coded signal to a TTL level bit stream for analysis by the Model 5500 internal logic. The BPV detector compares the output of the Data Detector to the AMI coding rule and passes information on violations of the rule to both the line Decoder and Counter Timer circuits which in turn initiate the count of BPV's displayed on the CRT.

In the B8ZS mode of operation the Line Decoder and Bipolar Violation Detector recognize the intentional Bipolar Violations found in B8ZS substitutions for strings of eight zeros.

All BPV's that are not associated with a valid B8ZS substitution are counted and displayed as BPV errors.

2.1.1 D4 Framing

The transmit and receive data may be either Framed or Unframed, as selected on the FORMAT Menu. In the Framed mode, the four test points accessible at the rear connector panel of the interface module provide "RX S BIT", "RX S BIT CLK", "TX S STB", and "TX MF SYNC" D4 Framing sync signals. The RX Frame Sync Logic provides D4 Framing Status information regardless of the Terminate/Bridge mode of the 5500. This feature is particularly useful in monitoring live traffic because it provides indication of the Framed/Unframed status of the monitored line and also identifies "F" Bit error, "S" Bit errors, loss of carrier (no bipolar pulses on the line) and "B2" ALARM (all Bit 2's = 0). This Framing Status data is combined and displayed as the "ALARM" parameter on the BERT menu.

Table 2-2 presents a summary of the "ALARM" display conditions:

Table 2-2. Alarm Display Conditions

DISPLAY	CONDITION
DISPLAY	CONDITION
ALRM.....	D4 Framed with no Framing Anomalies
ALRM.....F	The letter "F" in right hand position indicates the signal is not D4 framed. If the "F" is intermittently displayed, it indicates Framing errors on a D4 signal.
ALRM .....C..	Loss of Carrier (No RX Signal)
ALRM ...S....	"S" Bit Errors (alternate 193rd D4 bits are called "S" Bits).
ALRM B2.....	"B2" or "Yellow Alarm", all Bit 2's (in each DS0 channel byte) are zero.
	NOTE: These status/alarm conditions may occur in combination; their positions will always be the same. For example, alarms indicating "yellow alarm", "S" bit errors, loss of carrier , and frame errors would yield a display of: ALRM B2.S.C.F

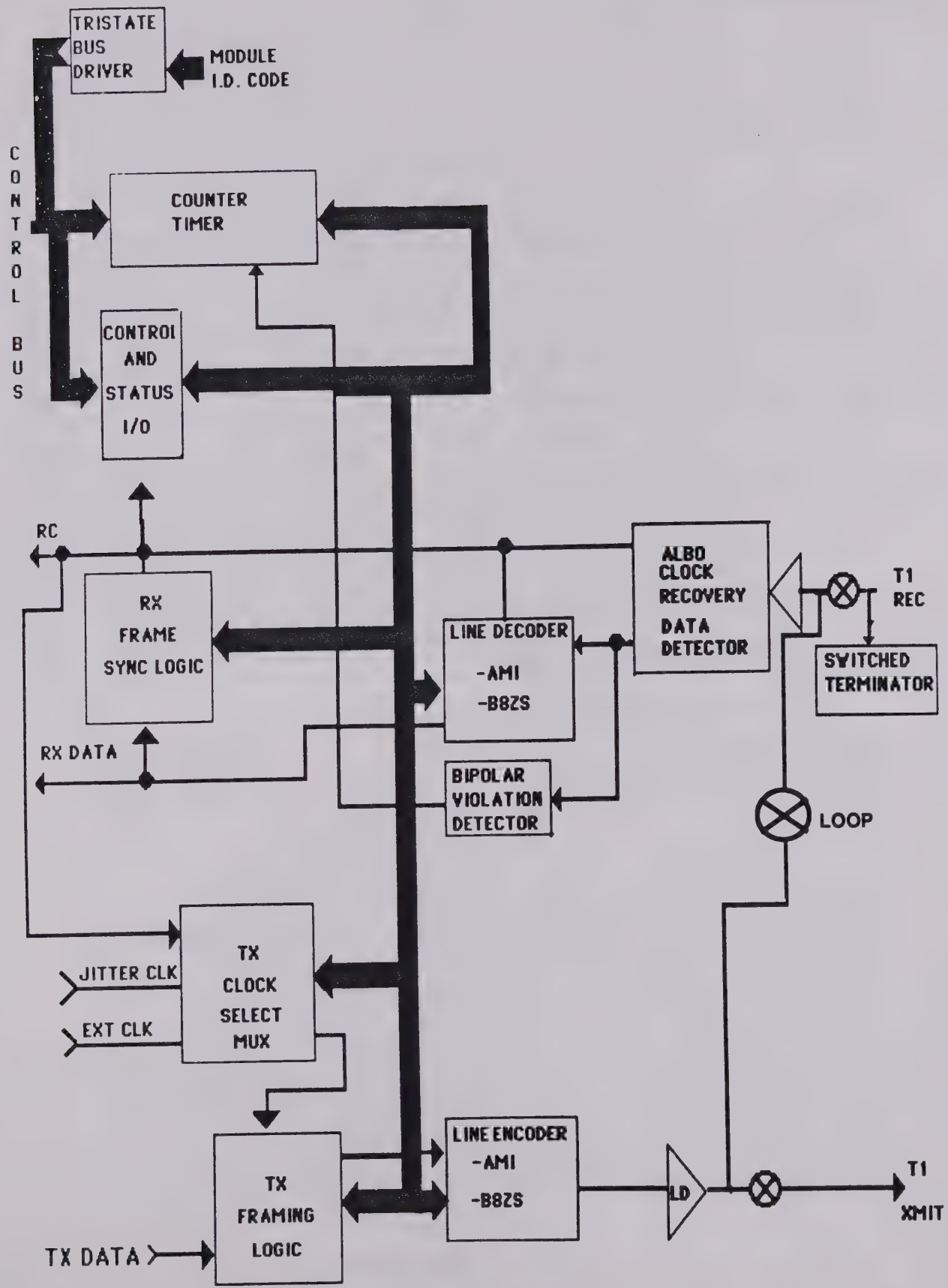


Figure 2-1. Model 5500-624 Interface Module Block Diagram

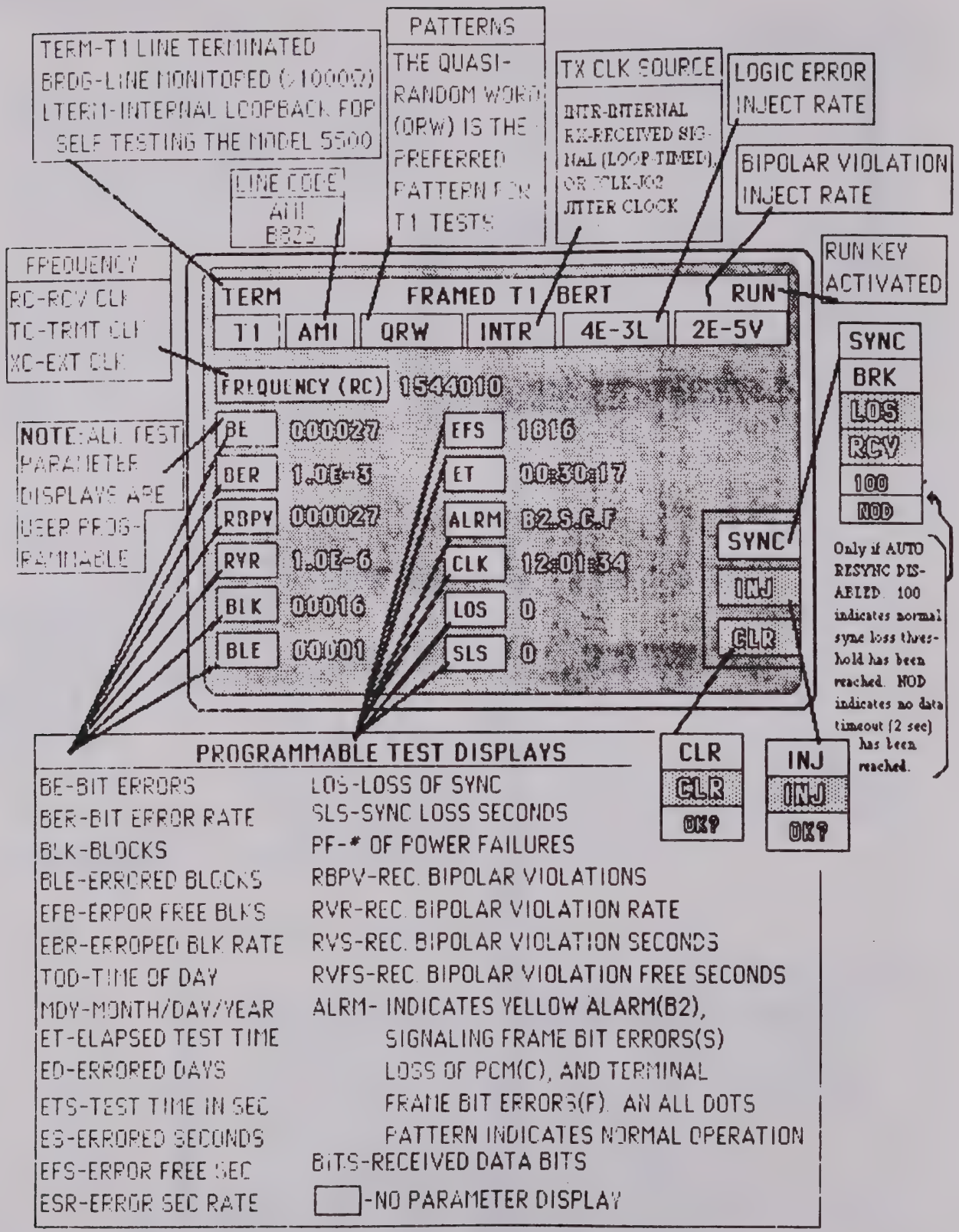


Figure 3-1. T1 Framed BERT Display

3.0 OPERATION

3.1 LOGIC/BPV ERROR INJECT/MEASURE

The 5500-624 Interface Module allows independent injection of BPV's and logic errors in the transmitted data. BPV inject rates are selectable from 2^{-3} to 1^{-7} and O (disable); logic error inject rates are selectable from 9^{-3} to 1^{-9} and O (disable). Rate control is independent, allowing injection of both BPV's and logic errors, only BPV's, only logic errors, or neither. Likewise, BPV's and logic errors are measured and displayed separately. While received logic errors are valid only when the selected pseudo random pattern is being received, the BPV parameter is valid for all received bipolar signals, including "live" traffic, as long as the proper line code (AMI or B8ZS) is selected.

3.2 TRANSMIT CLOCK SOURCE

The 5500-624 module allows three different clock sources to be used for transmit timing:

o Internal Clock (5500 1.544 Mhz Crystal Clock)

o Rx (Clock recovered from Rx received data input)

o Jitter (Jitter clock source from the JO2 Jittter Option Board).

Normal operation requires use of the Internal Clock. The Rx clock can only be used when the Receive Data Timing source is independently or "network" timed (Selection of Rx clock source when the 5500 transmit data is looped back to the 5500 receiver will not operate properly; in that mode the clock recovery circuit would in effect be chasing itself and would be very unstable and out of tolerance).

The Jitter clock source is used only when the JO2 Jitter option board is injecting jitter into the transmitted data output.

Clock source selection is via the FORMAT menu.

3.3 BERT FORMAT DEFINITIONS

Table 3-1 presents the T-Carrier BERT Format definitions that are unique to the Model 5500-624 Interface Module.

3.4 BER TEST ASSISTANCE

Table 3-2 presents a list of possible proablem areas if the Model 5500 does not achieve synchronization with the device under test.

Table 3-1. BERT Format Definitions

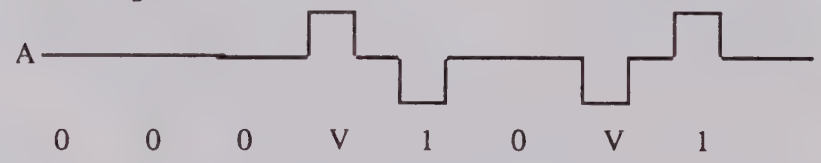
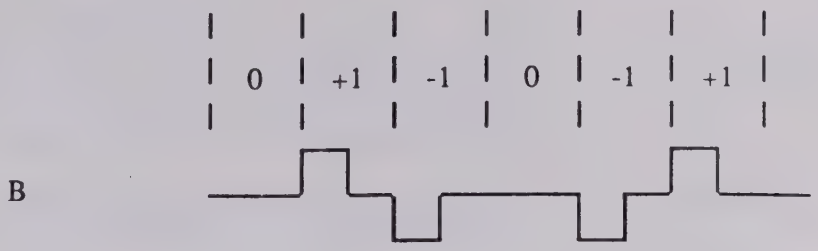
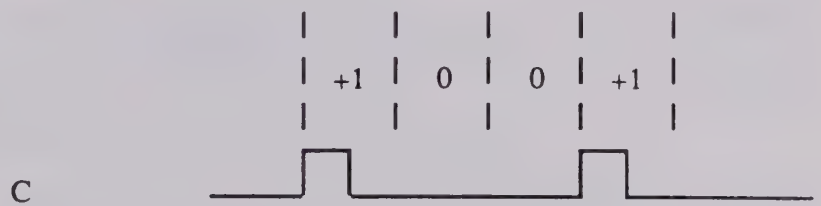
ITEM	DEFINITION
LINE RATE	This block displays the line rate as T1, T1C, or T2 for U.S. systems or 2.048 and 8.448 Mbps for CCITT G.703 modules. This is not a selectable parameter but is fixed by the interface module inserted into the Model 5500. It is a convenience item to remind the operator of the rate at which the Model 5500 is testing.
LINE CODE	The line code of the T-Carrier system under test may be selected by moving the half intensity block over the LINE CODE window and using the SELECT keys to choose the options. The options are: T1 AMI or B8ZS T1C AMI or B8ZS T2 AMI or B6ZS 2.048 Mbps AMI or HDB3 * * 2.048 Mbps G.703 modules are set for HDB3 at the factory. A DIP switch on the module allows selection of AMI coding. The Alternate Mark Inversion (AMI) or Bipolar line code is the line code currently in use in the U.S. on all T1 baseband source code into AMI line code. Note that successive MARKS (1's) always alternate in polarity. A new format, Bipolar 8 Zero Substitution (B8ZS), is being considered for T1 in order to remove the restrictions on the number of successive SPACES (0's) which AMI places on the source coder. While not in actual use at the present time, this line code may become the future standard. An example of a B8ZS coded signal is provided in figure A.  Assuming the last 1 transmitted was a positive "one". The polarities of the substituted word are simply reversed if the last "one was negative. 0 0 0 0 0 0 0 0 original word 0 0 0 +1 -1 0 -1 +1 substituted word BPV's always occur at the 4th and 7th bit positions of the substituted word. The line code used by T2 carrier systems is B6ZS which is similar to the B8ZS code previously discussed but which limits strings of 0's to less than 6. In this case a block of six consecutive zeros is substituted by the sequence "0 + - 0 - +" if the preceding mark was positive, or "0 - + 0 + -" if the preceding mark was negative (+ or - represents a positive or negative mark). An example of B6ZS coding is shown in figure B.

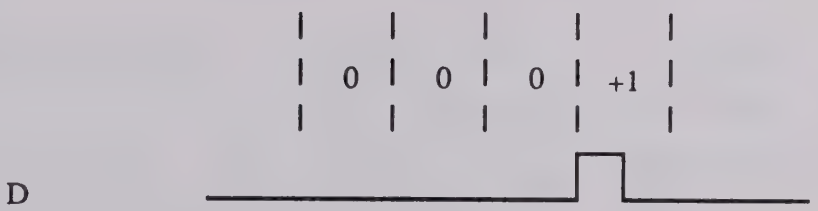
Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION



Finally, High Density, Bipolar 3 Zero Substitution (HDB3) line coding is used in European T-Carrier systems at 2.048 MBPS and 8.448 MBPS line rates. An example of this coding format is shown if figures C and D. (Preceding violation was negative and preceding pulse was negative in figure C and the preceding violation was negative and the preceding pulse was positve in figure D.)





The HDB3 coding process generates positive and negative marks alternately each time a binary logical 1 condition occurs within the message signal. However, unlike AMI coding, the maximum number of consecutive zeros is limited to a value of 3. If a series of 4 consecutive zeros does occur, the 4th zero is replaced by a mark referred t as a VIOLATION. The violation mark is always inserted with the same polarity as the preceding mark. This identifies the departure from the AMI scheme and indicates the occurrence of the violation.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
	In theory, if additional safeguards were not taken, it would be possible for several violations to have an identical polarity, and thus introduce a DC component into the signal. To overcome this problem, the coder continuously monitors the polarity of the last violation (may have been many bits earlier in the data stream) and the polarity of the last mark. The coder then forces the first bit of the 4-bit substitution sequence to a one or a zero, whichever is required, to allow the violation in the fourth bit position to be of opposite polarity to the previous violation.
PATTERN	The pattern choices from the regular FORMAT are all present in T-Carrier FORMAT, but the most useful patterns for T-Carrier testing are:
QRW QUASI-RANDOM WORD	A pattern of (2^20)-1 bits long which has built-in suppression of strings of 0's greater than 14. This pattern is the industry standard for T1 and T1C testing. (2^15)-1: A pseudo-random sequence used in European CCITT G.703 BER testing and jitter testing. (2^20)-1: A pseudo-random sequence of the same length as the QRW, but without the 14 zero suppression. Useful at T2 and for CCITT testing.
MARK	An all 1's pattern which may be used to simulate the "idle" pattern sent out by digital channel banks in an alarm condition.
USER	This is a user definable pattern of up to 135 characters (1080 bits) which could be used to send out patterns with more than 14 zeros or any other pattern a user may want to transmit.
T1 SET	This pattern sends out the standard T1 Channel Service Unit (CSU) loopback code (10000) to cause a remote CSU to loopback for test purposes. This code should be transmitted for 5 seconds before the CSU will loopback to prevent false loopbacks.
T1 RESET	This pattern sends out the standard T1 CSU reset code to return a CSU in loopback to normal operation. The code (100) should be sent out for 5 seconds to reset CSU loopback.
BPV INJ RATE	The user may select any rate of injection of Bipolar Violations from 2^{-3} to 1^{-7} violation/bit. The rate is selected by changing the mantissa from 0 to 9 (a 0 disables the inject function) first and then moving the half intensity block to the right and changing the exponent from -3 to -7 as desired. The select keys or the HEX keypad can be used. A common rate is 1^{-3} which is useful in checking automatic protection switches. Pressing the INJ soft key on the main BERT display activates BPV Injection unless there is a "0" in the BPV inject rate mantissa.
LOGIC ERR RATE	Logic errors are what telephone companies call bit errors to distinguish them from BPV's. This rate of bit error injection is selectable from 9x10-3 to 1x10-9 errors/bit. The errors (and bipolar violations) are uniformly spaced throughout the bit stream when the INJ soft key is pressed. Note that the user is free to have either logic errors or BPV's or both injected.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
CLOCK SOURCE	The user may select from three alternatives depending upon what simulation is being attempted. When the Model 5500 is acting as the generator of the T- Carrier it is normal to choose INTERNAL timing so that the Model 5500 is the master clock. This would be the case whenever any loopback testing is performed. The "RX" or Receive Clock choice allows the user to operate a 5500 in what is called a loop timed mode. That is, the Model 5500 derives clock from the received bit stream and uses this to time its transmitter. This is useful if, for example, the user is making an end to end bit error test with Model 5500's at each end. In this case one of the test sets should be on INTERNAL (acting as the master clock) and the other should be set to RX. The final option available is USER which allows the operator to supply a TTL clock to the rear panel BNC connector. The clock supplied must be at the nominal bit rate of the module being used (i.e. 1.544 MHZ for T1 module, 6.312 MHZ for T2, etc..), and should be at least + 30ppm accurate.

Table 3-2. BER Test Assistance

SYMPTOM	POSSIBLE CAUSE
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Verify that BRIDGE mode in T- Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units.
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when test set stops. This is normal operation.
Model 5500 display errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. NOTE: T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.

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Model 5500-628
DS1 (T1) Interface Module

The Model 5500-628 DS1 (T1) Interface Module enables the Model 5500 to test all types of T1 Carrier equipment with D4, ESF (Extended Super Frame), or SLC®96 framing (and also unframed T1 equipment). The line format is selectable for either AMI or B8ZS. The module includes a high performance ALBO/Clock Recovery circuit with wide dynamic range (+6dBdsx to -27dBdsx) and exceptional jitter tolerance (>10 UI peak-to-peak @600Hz, QRW pattern). The receiver may be operated in the BRIDGE, MONITOR, or TERMINATE modes.

The Model 5500-628 features extensive test capabilities for monitoring and troubleshooting "live traffic" circuits. Model 5500-628 test measurements are included in table 1-1.

Table 1-1. Model 5500-628 Test Measurements.

Measurement		D4	ESF	SLC"-96	Unframed
FBE	Frame Bit Errors	X	X	X	
FBER	Frame Bit Error Rate	X	X	X	
FBES	Frame Bit Errored Seconds	X	X	X	
FEFS	Frame Bit Error Free Seconds	X	X	X	
FLOS	Frame Loss of Sync (count)	X	X	X	
FLS	Frame Loss Seconds	X	X	X	
CRCE	Cyclic Redundant Check Errors		X		
CRES	CRC Errored Seconds		X		
CEFS	CRC Error Free Seconds		X		
CRER	CRC Error Rate		X		
15Z	>15 (consecutive) Zeros (events)	X	X	X	X
15ZS	>15 Zeros Seconds	X	X	X	X
BALS	Blue Alarm Seconds	X	X	X	X
YALS	Yellow Alarm Seconds	X	X		

Table 1-1. Model 5500-628 Test Measurements (Cont.).

Measurement		D4	ESF	SLC"-96	Unframed
FREQ	Frequency of RX Signal	X	X	X	X
LINE	Line Level with JO2 option				
	Volts Peak-to-Peak	X	X	X	X
	Pos. Peak, and	X	X	X	X
	Neg. Peak	X	X	X	X
%1SD	Percent One's Density	X	X	X	X
RBPV	Rx Bipolar Violations	X	X	X	X
RVR	Rx Violation Rate	X	X	X	X
RVS	Rx Violation Seconds	X	X	X	X
RVFS	Rx Violation Free Seconds	X	X	X	X
CSLP	Clock Slips (TX-RX clock pulses); TX jack serves as secondary receiver for clock slip reference timing when 628 module is in BRIDGE mode.	X	X	X	X
WND+	Wander "plus" = Maximum (peak hold) positive excursion of clock slips count measured in clock pulses (unit intervals).	X	X	X	X
WND-	Wander "minus" = Minimum (peak hold) negative excursion of clock slips count measured in clock pulses (unit intervals).	X	X	X	X

NOTE

The WND+ and WND- measurements are a direct indication of the maximum amplitude of low frequency phase jitter ("WANDER") and the minimum rate-buffer size required to avoid buffer overflow or underflow (and associated frame slips, sync breaks, etc.). The external clock input to the 628 module (accessible via the module 40 pin test connector with optional 5500-628TP cable) may be designated as the reference clock for slip/wander measurements simply by selecting EXT CLK as the CLOCK SOURCE on the FORMAT menu. Connection of the appropriate TTL level 1544000 Hz Stratum 1 reference clock to the EXT CLK input allows CLOCKSLIP and WANDER measurements relative to the network primary timing source.

1. In addition, the Model 5500-628 module provides the following features which may be particularly useful for "live traffic" diagnostic testing.

   a. "LOOP TIMED"/"NOT LOOP TIMED" indication based upon absence or presence of phase slips between the measured TX reference clock and the measured RX clock (threshold is +/- 40UI).

b. JO2 JITTER OPTION: Jitter measurement with spectral analysis for any T1 signal, in BRIDGE or MONITOR modes, D4, ESF, SLC®96, or unframed.

c. "ALARM" status indication of BLUE ALARMS, YELLOW ALARMS, S BIT ALARMS, Low Level Carrier, and FRAME ALARMS with automatic time stamped print outs of alarm events start and end.

d. ESF and SLC®96 data link access for monitoring and/or sending data link messages with a Phoenix Model 1500 analyzer/data trap or similar device.

2. The 5500-628 Module facilitates special "THRU" mode testing which allows the 628 module to be placed in series with a T1 circuit to:

a. Remove phase jitter from live traffic (with JO2 option).

b. Add phase jitter to live traffic (with JO2 option).

c. Inject bit errors (data or framing) in live traffic.

3. The 5500-628 also facilitates the following diagnostic error injection modes:

a. Frame bit error injection.

b. S bit error injection (D4).

c. CRC error injection (ESF).

d. Data error injection (in all "THRU" data and in originating ESF data bits after CRC6 calculations--allowing verification of receiver CRC error detection correlated with BERT error detection).

e. BPV injection after line coding.

f. Independent logic error injection (in BERT pattern before framing).

2.0 TEST MODES

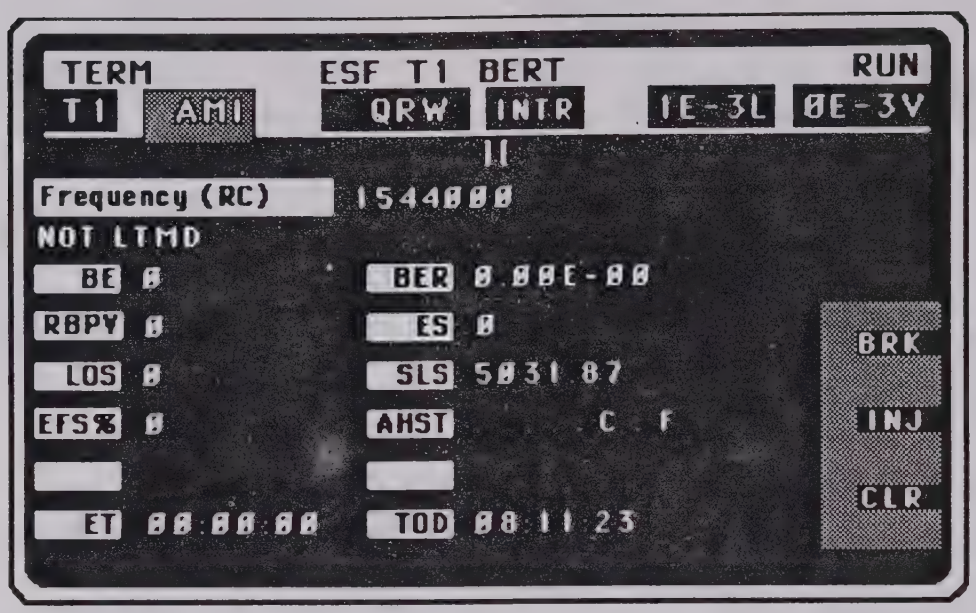
2.1 MONITOR T1 SIGNAL

On the Format menu, figure 2-1, select the appropriate termination mode; Bridge, Terminate, or Monitor, using the following guidelines:

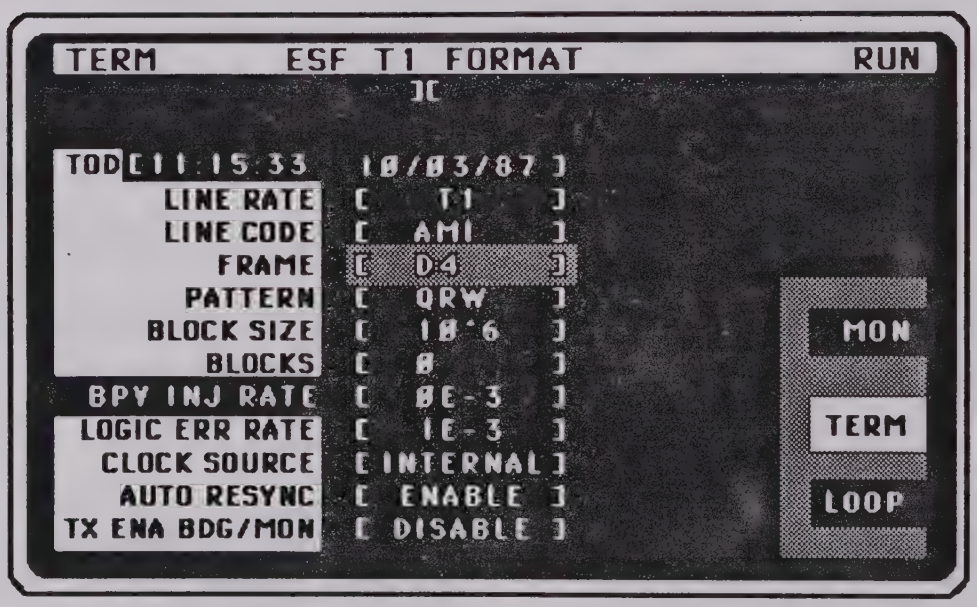
> ***NOTE***
>
> The top soft key is the MON key. Activate this key to the "highlighted" state for "MONITOR" mode. Deactivate the MON key to the "not highlighted" state to return to the highlighted BRDG or TERM mode. The middle softkey is an alternate function TERM/BRDG key. Activate this softkey to change from the displayed mode (i.e. TERM) to the alternate mode (i.e. BRDG).

BRDG mode (BRIDGE high impedance termination option; SAFEST for the curious when wishing to avoid interference with the monitored circuit).

TERM mode (terminates the RX pair with 100 ohms -- to be used only when the monitored circuit "terminates" at the Model 628 test interface -- normally used only in out-of-service testing when the test set is sub-

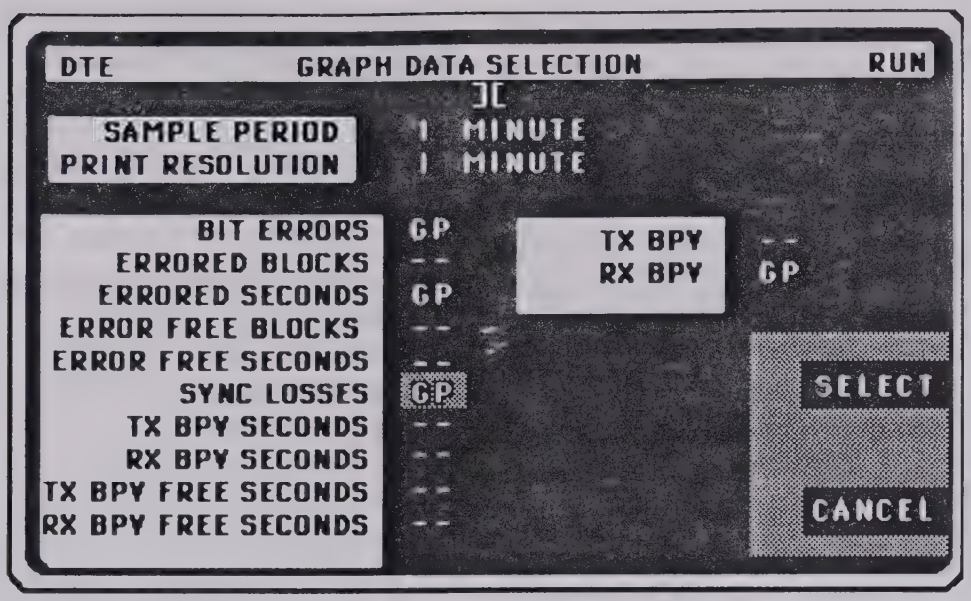


ESF T1 BERT Display

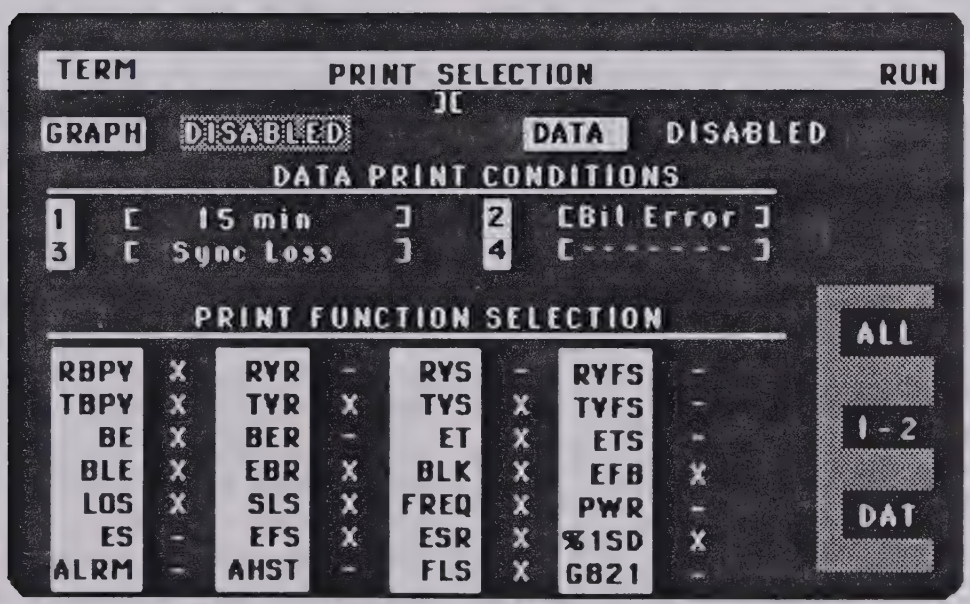


ESF T1 BERT Format

ESF T1 Menus
Figure 2-1 Sheet 1 of 2



ESF T1 Graph Data Selection Menu



ESF T1 Print Selection Menu

ESF T1 Menus
Figure 2-1 Sheet 2

stituted for the normal network terminating device).

MON mode (MONITOR mode is specifically for DSX panel test access via a standard DSX "MONITOR" jack which provides two 430 ohm resistors in series with tip and ring -- in this mode the test set will terminate the RX pair with 100 ohms, resulting in 20dB attenuation of the resistor isolated monitor signal. The resistors minimize circuit interference which might otherwise result from the test set load impedance, test probe contact bounce transients, or an improper test connection to a transmitter instead of a receiver.) The MONITOR mode envokes a 20dB amplifier (voltage gain of 10) to compensate for the 20dB attenuation of the 430 ohm resistors. The BRIDGE mode of termination is compatible with resistor isolated MONITOR jacks (by virtue of high impedance termination and 628 receiver amplitude tolerance); however, the MONITOR mode is more appropriate when remote test access requires test lead length in excess of fifteen feet. MONITOR jack remote test access wire lengths in excess of 2000 feet may be accommodated by using standard, Z0=100 ohm, wiring --with the 628 module MONITOR mode providing the 100 ohm termination, 20dB amplifier and ALBO equalization of the extended Monitor circuit.

NOTE

In the "MONITOR" mode, the monitored circuit will be bridged with a 100 ohm load with the expectation that series 430 ohm isolating resistors are externally provided. The line level measurements (with the JO2 option) will be accurate only when the proper BRDG/MONITOR mode is selected to match the condition at the test access connection (i.e. if series 430 ohm resistors are present, select MON; if the series 430 ohm resistors are absent, select BRDG).

2.2 CONNECT THE 628 MODULE TO THE CIRCUIT(S) OF INTEREST

The RX INPUT jack is a "bantam" type, 3 conductor (tip, ring, and sleeve) miniature phone jack. Tip and ring are connected to the primary winding of the 628 receiver isolation transformer via series relay contacts. The relay contacts are normally closed in all modes except when "LOOP" is enabled. The sleeve is connected to the test set "ground" circuit for shield termination.

The TX OUTPUT jack is likewise connected, tip and ring, to the secondary winding of the 628 transmitter output transformer via series relay contacts. The relay contacts are normally closed only in the "TERM" mode and open in the "BRDG" and "MON" modes (and open anytime "LOOP" is enabled). The "TX ENA BRDG/MON" ENABLE/DISABLE option on the Format menu allows the TX relay to be enabled or disabled in the Bridge and Monitor modes. The sleeve is connected to the test set "ground" circuit for shield termination.

The outboard center taps of the TX and RX transformers may be connected via a small two position rotary switch for the purpose of providing a simplex current path for "wet" repeatered span lines when the 628 module terminates the span. This switch is accessible through the bottom cover of the 628 module when removed from the chassis. The switch positions are clearly labeled and a small, flat blade adjustment tool (screwdriver) is provided with the module.

An auxilary 15 pin "D" type female connector is wired in parallel with the TX and RX bantam jacks. Any combination of connections may be employed as desired, including bridging of circuits using both types of connectors, as long as the RX tip/ring circuits and TX tip/ring circuits are completed. Phasing of the tip/ring connections to a balanced T1 circuit may be arbitrary with no effect on 628 module performance. The pin outs of the 15 pin connector are as follows:

pin 1 TX TIP (OUTPUT)
pin 9 TX RING (OUTPUT)
pin 3 RX TIP (INPUT)
pin 11 RX RING (INPUT)
pin 4 GROUND (SHIELD TERMINATION)

The TX tip and ring are always connected to an auxilary clock recovery circuit in the 628 module. This circuit constantly monitors the clock frequency of the bipolar T1 signal present on the TX tip/ring circuit. In the "TERM" mode this T1 signal is generated by the 628 module at the frequency (and phase) of the selected clock source. In all other modes the TX OUTPUT jack may be used as a high impedance (>1000 ohms) bridging monitor circuit for the purpose of measuring the frequency and phase of any T1 bipolar signal relative to the frequency and phase of a second T1 bipolar signal connected to the RX INPUT jack. By selecting the "TERM" mode and "EXT CLK" clock source, the external TTL clock will be selected as the reference clock for the clock slip and wander measurements of the 628 module.

2.3 SELECT FRAMING: D4, ESF, SLC®96 or DISABLED (unframed)

Observe the "ALRM....." parameter status on the BERT menu.

ALRM.....FIndicates a FRAME alarm (out of frame sync).

ALRM..... Indicates no alarms (in frame sync, test set verification of selected framing).

ALRM...S.... Indicates frame sync with "S bit" framing errors. The S bits are the frame bits in frames 2, 4, 6, 8, 10 and 12 whose purpose it is to identify the location of frames 6 and 12 which contain robbed bit signalling (the signalling bits are substituted for the least significant bits in each of the 24 digitized voice channel time slots). In D4 framing the S bit sequence is 111000 with the first "1" indicating the beginning of frame 6 (containing the "A" signalling bits) and the first "0" indicating the beginning of frame 12 (containing the "B" signalling bits). The S bit alarm will be indicated only for D4 or SLC®96 framing (there are no S bits in ESF). The only distinguishing difference between D4 and SLC®96 frame bit patterns is the S bit sequence. In D4, the S bit sequence is fixed at 111000; in SLC®96 the S bit positions are used for a network control data link alternating with the S bit frame aligning sequence. The S bit alarm activity in the SLC®96 mode simply confirms data link activity in the S bit positions of the frame bit sequence.

ALRM...C.....Indicates low level carrier (input signal level is approx. -27dBdsx or less).

ALRM.Y.....Indicates YELLOW ALARM

ALRM...B....F Indicates a BLUE ALARM (unframed all ones), and causes BALS to increment.

ALRM...B.....Indicates a "FRAMED BLUE" condition (framed all ones); does not cause BALS to increment because this is not a true BLUE ALARM condition.

3.0 CLOCK SOURCE MODES (Including "THRU" data modes)

There are 7 possible selections for the source of the transmit clock timing, refer to table 3-1, for the "TX OUTPUT" of the 628 module (4 without the JO2 Jitter Option

Table 3-1. Model 5500-628 Clock Sources.

CLOCK SOURCE	DESCRIPTION
INT CLK	Internal Oscillator (main chassis/not in module) Select INT CLK for any standalone equipment testing and anytime loop timing is not appropriate (someone in the net work must originate the clock; everyone cannot slave to recov ered clock).
RX CLK	"RX INPUT" recovered clock Select RX CLK anytime the "TX OUTPUT" is required to be "loop timed" to the "RX INPUT" clock.
EXT CLK	TTL input via pins 15 (EXT CLK) and 36 (RETURN) of the 40 pin "TEST ACCESS I/O" connector. Connect any TTL external clock source @ 1544000+/-300 Hz for frequency tolerance testing of receivers, repeaters, etc. Connect any TTL precision clock, or network stratum 1 clock, etc., for use as: A) "TX OUTPUT" timing clock, and/or B) CSLP reference clock.
JIT CLK	The JO2 OPTION modulates the internal clock source as specified via the Jitter Option Menu. The amplitude and fre quency of phase modulation (and modulation wave shape - sine, triangle, or external modulation source) may be controlled to evaluate the jitter tolerance of network components.

Table 3-1. Model 5500-628 Clock Sources (Cont.).

CLOCK SOURCE	DESCRIPTION
THRU	"RX INPUT" bit stream is retransmitted at "TX OUTPUT" with all data bits, frame bits, data link bits, bipolar violations, etc. unaltered. This mode may be used to provide an in line repeater function (ALBO phase compensation, clock recovery, & retransmission of a nominal 6Vpeak-to-peak signal with 10%-30% trailing edge overshoot per Pub 62411). This mode also provides for injec tion of data errors, frame errors, etc. in live traffic for evaluation of error tolerance of command/response protocols, error check ing algorithms, packet switching protocols, etc. (when the standard BERT pseudorandom test patterns are inappropri ate).
THRU-J	Same as "THRU" above except the phase jitter (up to 10 unit intervals peak-to-peak) of the recovered "RX INPUT" clock is at tenuated by approx. 40dB at 120 Hz (and above) to a level of less than .1 unit intervals peak-to-peak. This de-jittered clock is then used as the "TX OUTPUT" clock source. This mode may be used to sectionalize jitter tolerance problems, especially when the standard BERT pseudorandom test pat terns are inappropriate and/or when extended out of service testing and troubleshooting is not permitted.
THRU+J	Same as "THRU" and "THRU-J" above except the "jitter attenu ated", recovered "RX INPUT" clock is phase modulated as specified via the JO2 jitter option menu, and then used as the "TX OUTPUT" clock source. This mode may be useful in characterizing the jitter tolerance margins (or shortcomings) of network components in "live traffic" situations.

4.0 SHARPSHOOTER™ ERROR INJECTION:

The error injection modes and capabilities of the 628 module are listed in table 4-1 (in each case the errors are injected in the 628 "TX OUTPUT" bipolar signal regardless of the source of the data,i.e. BERT pattern, User Pattern, RX data in "THRU" mode; and/or the source of the transmit clock, i.e. INT CLK, EXT CLK, RX CLK, JIT CLK (INTERNAL PHASE JITTER CLK), THRU CLK, THRU-J (DE-JITTERED THRU CLK), THRU+J (Jitter modulated average THRU CLK).

Table 4-1. Error Injection Modes.

FRAME	CLK	BPV INJ	FBIT INJ	SBIT INJ	DATA INJ	CRC INJ
D4	INT	X	X	X		
D4	EXT	X	X	X		
D4	RX	X	X	X		
D4	THRU	X	X	X	X	
D4	JIT(JO2)	X	X	X		
D4	THRU-J(JO2)	X	X	X	X	
D4	THRU+J (JO2)	X	X	X	X	
SLC®96	INT	X	X			
SLC®96	EXT	X	X			
SLC®96	RX	X	X			
SLC®96	THRU	X	X		X	
SLC®96	JIT(JO2)	X	X			
SLC®96	THRU-J (JO2)X	X	X		X	
SLC®96	THRU+J(JO2)X	X	X		X	
ESF	INT	X	X		X	X
ESF	EXT	X	X		X	X
ESF	RX	X	X		X	X
ESF	THRU	X	X		X	X
ESF	JIT (JO2)	X	X		X	X
ESF	THRU-J (JO2)X	X	X		X	X
ESF	THRU+J (JO2)	X	X		X	X
"UNFRAMED":						
DISABLE	INT	X				
DISABLE	EXT	X				
DISABLE	RX	X				
DISABLE	THRU	X				X
DISABLE	JIT(JO2)	X				
DISABLE	THRU-J (JO2)X	X				X
DISABLE	THRU+J (JO2)	X				X

4.1 ERROR INJECTION TEST PROCEDURE

The following test exercises demonstrate the operation of the various error injection modes and provide reference test parameters for validation of test set performance. Unless otherwise specified, all tests are based on operation of the 5500 in "LOOP" or with an external jumper cable from TX to RX. The error injection mode is selected by scrolling the parameter label field in the location normally reserved for "BPV INJ RATE" on the FORMAT menu. This is accomplished by first moving the cursor up or down in the right hand column and then left into the (dark background) INJ mode field. The available inject modes are automatically restricted to those appropriate for the selected combination of FRAME and CLOCK SOURCE modes.

4.1.1 BPV Inject

Select any FRAME mode, including DISABLE.

4.1.1.1 High Range:

Set BPV INJ RATE = 5E-3;
Enable INJ;
Double-Activate CLR/OK?;
Verify RVR converges to 5.00E-3.

4.1.1.2 Low Range:

Set BPV INJ RATE = 5E-6.
Double-Activate CLR/OK?;
Verify RVR converges to 5.00E-6.

4.1.1.3 Single Error Inject

Disable INJ;
Double-Activate CLR/OK?;
Enable then quickly disable INJ;
Verify RBPV = 1.

4.1.2 FBIT ERROR INJECT

Select any FRAME mode, excluding DISABLE.

4.1.2.1 Set FBIT INJ RATE = 5E-3;

Enable INJ;
Double-Activate CLR/OK?;
Verify FBER converges to 5.00E-3.

4.1.2.2 Single Error Inject

Disable INJ;
Double-Activate CLR/OK?;
Enable then quickly disable INJ;
Verify FBE = 1.

4.1.3 SBIT ERROR INJECT

Select D4 FRAME mode.

4.1.3.1 Set SBIT INJ RATE =1E-4

Enable INJ;
Double-Activate CLR/OK?;
Verify ALRM....S....Is displayed for approx.
1 sec. every 2.5 sec.
"ALRM...S..." should alternate with "ALRM....." 4 times in 10 sec.

Using a Model 5575 MicroBERT (Model 5500 does not count "S" bit errors or measure "S" bit error rate):
Verify SBER = 1E-4.

4.1.3.2 Single Error Inject

Disable INJ;
Double-Activate CLR/OK?;
Enable then quickly disable INJ;
Verify ALRM...S... is displayed for approx. 1 sec.

Using a Model 5575 MicroBERT, verify SBE increments by only 1 count.

4.1.4 CRC ERROR INJECT

Select ESF FRAME mode.

4.1.4.1 Set CRC INJ RATE = 5E-3;

Enable INJ;
Double-Activate CLR/OK?;
Verify CRER converges to 5.00E-3.

4.1.4.2 Single Error Inject

Disable INJ;
Double-Activate CLR/OK?;
Enable then quickly disable INJ;
Verify CRCE = 1.

4.1.5 DATA ERROR INJECT [THRU MODES]

> ***NOTE***
>
> This mode allows errors to be injected in the data bit positions of the received "RX INPUT" signal which is to be re-transmitted (with injected errors) via the "TX OUTPUT". In this mode, errors will be injected only in the data bit positions -- No errors will be injected in the frame bit, S bit, datalink bit, or CRC bit positions.

4.1.5.1 D4, SLC®96, or disabled framing in 'THRU" modes (refer to para. 4.1.5.2 for special ESF mode)

Connect any external T1 source to the "RX INPUT" and select the appropriate "Frame" mode, and Termination mode.

Monitor the "TX OUTPUT" with a second test set

4.1.5.1.1 Select CLOCK SOURCE = THRU or THRU-J [remove jitter] or THRU+J [add jitter] as desired.

Set DATA INJ RATE = 5E-3;
Enable INJ;
On a second test set monitoring the TX OUTPUT, verify BER converges to 5.00E-3.

> ***NOTE***
>
> The "THRU" mode 5500 will measure and display the "BER" of the received "RX INPUT" signal; the injected errors @ a rate of 5.00E-3 may be observed via a second test set monitoring the "TX OUTPUT" signal.

Verify no FBIT, SBIT, or CRC errors are injected.

In the THRU+J and THRU-J modes, a BPV will occur simultaneously with the injected data error (allowing scope sync on the error via a BPV test point). A BPV will not occur with injected data or frame errors in any other Model 5500 clock source modes.

4.1.5.1.2 SINGLE ERROR INJECT

Disable INJ;
Enable then quickly disable INJ;
Verify BE = 1 (on a second test set monitoring "TX").

4.1.5.2 ESF DATA ERROR INJECT FOR CRC PERFORMANCE EVALUATION:

> ***NOTE***
>
> A special data error inject mode is provided for ESF framing. "D INJ (CRCrate)" causes data errors to be injected to achieve a specific detected CRC error rate. If the target receiver CRC checking algorithm is operating correctly, it will verify the anticipated CRC error rate.

"D INJ (CRCrate)" is available in all ESF modes, including originating BERT patterns, User Patterns, and "LIVE" thru traffic.

4.1.5.2.1 Set D INJ (CRCrate) = 5E-3;

Enable INJ;
On a second test set monitoring the TX OUTPUT of the "THRU" test set:
Verify CRER converges to 5.00E-3;
Verify BER converges to 1.09E-6.

> ***NOTE***
>
> The "THRU" mode 5500 will measure and display the "CRER" and "BER" of the received "RX INPUT" signal; the injected errors @ a rate of 5.00E-3 may be observed via a second test set monitoring the "TX OUTPUT" signal.

Verify no FBIT or SBIT errors are being injected.

In the THRU+J and THRU-J modes, a BPV will occur simultaneously with the injected data error (allowing scope sync on the error via a BPV detector test point). A BPV will not occur with injected data or frame errors in any other 5500 clock source modes.

4.1.5.2.2 Single Error Inject

Disable INJ;
Double-Activate CLR/OK?;
Enable then quickly disable INJ;
Verify CRCE = 1;
Verify BE = 1.

5.0 >15ZTEST

Set FRAME = D4 or ESF or SLC®96;
Set LINE CODE = AMI;
Set PATTERN = QRW;
Activate TERM and LOOP ;
Verify 15Z = 0.
Verify 15ZS = 0.
Set PATTERN = 2^20-1;
Verify 15Z increments @ approx. 12 counts per second.
Verify 15ZS increments 1 count per second.

6.0 FLOS and CARRIER ALARM TEST

Set FRAME = D4 or ESF or SLC®96;
Activate TERM;
Externally jumper "RX INPUT" to "TX OUTPUT"
Double-Activate CLR/OK?;
Verify "ALRM....."
Verify FLOS = 0.
Quickly disconnect RX cable (to minimize contact bounce);
Verify FLOS = 1;
Verify "ALRM....C.F" (Low level carrier and loss of frame sync).

7.0 YELLOW/BLUE ALARM TEST

Set FRAME = D4
Set LINE CODE = AMI;
Set PATTERN = ALT;
Activate TERM and LOOP;

ALRM = "Y....." indicates phasing of the ALT pattern
relative to the frame bit is such that bit 2 of each of the
24 "channel" bytes is a "0" -- which constitutes a yellow alarm.
If ALRM = ".....", de-select and re-select ALT pattern
several times until the proper phasing is achieved [50%
probability of YELLOW ALARM each time ALT pattern
is re-selected].

Verify YALS increments 1 count per second (Yellow Alarm seconds).

> ***NOTE***
>
> The 628 module does not recognize a YELLOW ALARM in the SLC®96 mode.
>
> The YELLOW ALARM condition for ESF is not the same as for D4. ESF YELLOW ALARM is an alternating 1111111100000000 pattern in the DATA LINK bits. The 628 will detect ESF YELLOW but will not transmit ESF YELLOW; therefore, an external source must be used to check this function.

Set PATTERN = MARK;

Verify "ALRM .B.....", indicating "FRAMED" BLUE ALARM (the absence of the "F" indicates frame sync i.e. frame alarm is off). The industry standard BLUE ALARM is "UNFRAMED ALL ONE'S"; However, some equipment will use FRAMED ALL ONE'S as an alarm or "SQUELCH" condition.

Verify BALS (BLUE ALARM seconds) does not increment.

Set FRAME = DISABLED;

Verify "ALRM ..B.....F", indicating BLUE ALARM (UNFRAMED ALL 1"s).

Verify BALS increments 1 count per second (BLUE ALARM seconds).

8.0 CLOCK SLIP, WANDER, NOT LOOP TIMED TESTS

CSLP [CLOCK SLIP] is a measure of the relative phase of the recovered "RX" clock and the recovered "TX" reference clock, measured continuously from the start of the test. A CSLP of +7 indicates that the "RX" clock has shifted by 7 unit intervals (1 unit interval = 1 clock period = 0.647 microseconds @ 1544000 Hz) relative to the phase of the "TX" reference clock. A clock recovery circuit extracts the clock rate of the "TX OUTPUT" bipolar signal for use as the reference clock for CSLP measurements. The WND+ (Wander positive) and WND- (Wander negative) parameters are the maximum and minimum values, respectively, of the CSLP measurements since the start of the test. These parameters may be especially useful in measuring worst case peak-to-peak WANDER relative to rate buffer overflow and/or underflow problems in multiplexer equipment; i.e. If a multiplexer is designed to accommodate 28 unit intervals peak-to-peak, WANDER, and the measured WANDER is greater than 28 unit intervals peak-to-peak, then sync breaks, controlled frame slips and related events may be expected. Clock slip rate may be derived from the CSLP data by monitoring the CSLP count at specific time intervals and calculating the rate of slip as "DELTA CSLP" divided by "DELTA TIME". As long as CSLP remains within the range of + or - 40 unit intervals, the LTMD (loop timed) indication will be displayed in the BERT

menu. When CSLP exceeds this range, the flashing NOT LTMD (not loop timed) indication will be displayed.

The 628 module employs a second, independent clock recovery circuit bridged across the "TX OUTPUT" jack which may be employed as a secondary receiver for the purpose of extracting a CSLP reference clock from any DSX level signal. This is accommodated by disconnecting the 628 module transmitter via the TX ENA BDG/MON [DISABLE/ENABLE] option available on the format menu. Alternately, this option permits the internal transmitter to be used simultaneously with the single receiver RX Bridge or Monitor test modes. This option affords complete remote control of the TX connect/disconnect function without external relay switching equipment.

CSLP, WND+, WND-, LTMD, Not Loop Timed test procedure:

Select TERM, MON, or BRDG, as appropriate, and
connect any external T1 source to the "RX INPUT"
Select "TX ENA BDG/MON" to enable;
Select CLOCK SOURCE = RX;
Select PATTERN = QRW (or anything but SPACE);
Select FRAME = (your choice);
Double-Activate CLR/OK?;
Verify CSLP = 0 (+ or - 1);
Verify WND+ = 0 (+ or - 1);
Verify WND- = 0 (+ or - 1).

Verify LTMD indication is displayed (upper left on BERT menu).

Select CLOCK SOURCE = INT;

Verify CSLP starts to increment positive (or decrement negative) at a uniform rate.

If CSLP is "+" POLARITY ; Verify "WND+" tracks CSLP, and
verify WND- remains @ 0 (+ or - 1).
If CSLP is "-" POLARITY; Verify "WND-" tracks CSLP,
and verfiy WND+ remains @ 0 (+ or -1).

Verify LTMD remains displayed until CSLP reaches a count
of +40 or -40, then changes to flashing "NOT LTMD".

9.0 TEST ACCESS CONNECTOR

A 40 pin Test Access Connector (use option cable 5500-628TP for access) provides the test points, clock inputs, clock outputs, jitter modulation and jitter demodulation access pins listed in table 9-1.

Table 9-1. Test Access Pin Connections.

FUNCTION	PIN NO.	DESCRIPTION
External Clock	15	TTL EXT CLK INPUT
External CLK RTN	36	CLK RETURN
Jittered TX CLK	13	Jitter Modulated TTL XMIT CLK
Jittered TX CLK RTN	16	CLK RETURN
Dejittered RX CLK	29	De-Jittered TTL RX Recovered CLK
Frame Alarm T.P.	5	TTL; 1=Frame Alarm, 0=Frame Sync.
RX BPV T.P.	25	TTL; Ø = BPV, 1=No Violation
RX CRC6 Error T.P.	26	TTL; Ø = CRCE, 1 = No CRCE
RX FBIT Error T.P.	8	TTL; Ø = FBE, 1 = No FBE
RX Superframe Sync T.P.	27	TTL; Logic Ø Pulse (Duration of last RXFrame)
RX Frame Sync T.P.	9	TTL; Logic Ø Pulse (193rd TX BIT).
TX Superframe Sync T.P.	28	TTL; Logic Ø Pulse (Duration of first TXframe)
TX Frame Sync T.P.	14	TTL; Logic Ø Pulse (193rd TX BIT)
Test Point Returns	34,35,38	Logic GND for T.P. Returns
*RX Data Link Out	10	RS-232 Data Link RD Output
*RX Data Link CLK Out	30	RS-232 Data Link RC Output
*TX Data Link In	31	RS-232 Data Link TD Input
*TX Data Link CLK Out	11	RS-232 Data Link TC Output
*Data Link RTN	7	RS-232 CKT GND
TX Jitter Mod Input	20	Analog Modulation in (JO2 Option)
TX Jitter Mod RTN	19	Analog Modulation in (JO2 Option)
RX Jitter Demod Out	17	Analog Demodulation out (JO2 Option)
RX Jitter Demod RTN	18	Analog Demodulation out (JO2 Option)

NOTE: All other pins are reserved for future use.

* Standard RS-232 "DCE" for direct connection to an external "DTE" device.

Model 5500-700

T-2 Interface Module

1.0 INTRODUCTION

The Model 5500-700 T-2 Interface Module enables the Model 5500 to test T-Carrier Systems operating at 6.312 Mbps rates (T-2) in accordance with the applicable Bell System and U.S. Telephone Association specifications. The module provides two output levels to simulate the 6.312 Mbps signals found at both terminal equipment and at the DSX-2 cross connect, as well as providing the capability to monitor the signal levels originating from both locations. The T-Carrier signals for T-2 are serial, bipolar (return-to-zero) pulses that utilize the Bipolar with six zero substitution (B6ZS) line code. The T-2 Interface Module provides this capability, and in addition, may be configured to provide the Alternate Mark Inversion (AMI) line code via switch selection on the module.

The Model 5500-700 T2 Interface Module enables the Model 5500 to generate and receive T2 serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consists of Western Electric Company type 310 compatible jacks for transmit and receive.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-700 Interface Module.

Table 2-1. Model 5500-700 Specifications

CHARACTERISTIC	SPECIFICATION
TRANSMITTER	
Pulse Rate	T2-6.312 Mbps ±33 ppm
Output Pulse Amplitude (user selectable)	DS2H-2.1V Peak ±10% DSX2-2.1V Peak ±10% in series with a 1000 ft. ABAM cable simulator (LBO)
Output Pulse Shape	DS2H-Rectangular, 78 ±8 nsec pulse width at 50 percent amplitude.
	DSX2-In accordance with AT&T compatibility bulletin No. 119 DSX2 pulse template.
Overshoot	Less than 10% of amplitude height.
Line Code	B6ZS of AMI (user selectable)
RECEIVER	
Input Level	DS2H - ±2.1v peak plus up to 2155 ft. ABAM cable.
	DSX2 - .2-7.3 dbm plus up to 1000 ft. ABAM cable.
Input Impedance	110 ohms ±5% terminated. >1000 ohms bridged.

2.1 FUNTIONAL DESCRIPTION

The Generator section (refer to figure 2-1) consists of a line encoder, a line driver, and a series 1000 ft. ABAM cable simulator (LBO) that may be selected via the switch on the T2 Interface Module panel. The LBO is placed in series with the line driver in the "DSX2" switch position. The line encoder can be configured to produce an AMI or B6ZS line code for the bit stream at the T2 rate.

The model 5500 T2 BERT Display and Format Menus (refer to figures 2-2 and 2-3) display the line code. When position 1, SW3, of the T2 Interface Module is in the "ON" position, these display areas will display "B6ZS" or "HDB3". When the switch is in the "OFF" position, these display areas will display "AMI" or B8ZS". Since T2 will only utilize AMI or B6ZS, the proper line code may be selected via the menu soft keys once the switch on the T2 Interface module has been placed in the desired position.

The receive section of the module contains two independent receivers. This configuration enables the Model 5500 to monitor both Receive pair and Transmit pair traffic for Bipolar Violations. The Receive input has a switchable line termination to enable it to receive input signals and terminate them in 110 ohms, as well as monitor signals in a Bridged mode. With the exception of the switchable impedance, each receiver is the same. The receiver section recovers and regenerates the signal at the DSX point or from terminal equipment. The clock recovery circuit (basically a phase locked loop) derives timing from the incoming bit stream and feeds it to the data detector, line decoder, and the Model 5500 internal logic. The Receive Clock and received Transmit Clock are both recovered in this manner.

The Data Detector accepts the output signal of the Receiver and combines it with the recovered clock to do the final reshaping and regeneration of the input which is then passed to the Line Decoder and Bipolar Violation Detector. The Line Decoder is set to AMI or B6ZS as appropriate and converts the line coded signal to a TTL level bit stream for analysis by the Model 5500 internal logic. The BPV detector compares the output of the Data Detector to the AMI coding rule and passes information on violations of the rule to both the line Decoder and Counter Timer circuits which in turn initiate the count of BPV's displayed on the CRT.

In the B6ZS mode of operation the Line Decoder and Bipolar Violation Detector combine to ignore intentional Bipolar Violations.

3.0 OPERATION

Selection of the line code is performed in the following manner:

1) Remove the top cover of the T2 Interface Module, held in place with four Phillips head screws.

2) Carefully separate the top PC board (T2 I/O Module Board) from the bottom PC board (T2 Control Board) and remove the transmit and receive cable connectors from the top PC board.

3) Configure SW3, position 1, for the desired line code. Select "ON" for B6ZS or "OFF" for AMI (refer to figure A below).

4) Reassemble the T2 Interface Module, taking care not to bend any of the pins on the connectors between the top and bottom PC boards.

NOTE: Switch positions other than SW 3, position 1, are shown for illustration **ONLY,** and may or may not represent the factory setting for your module.

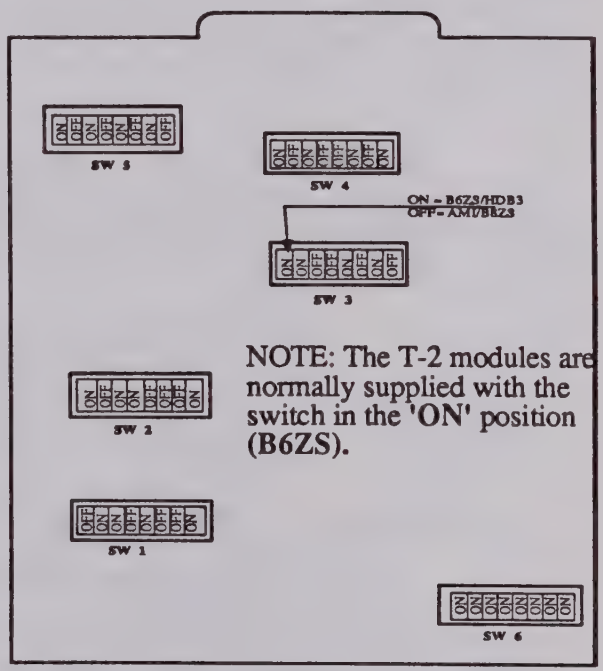


Figure A

3.1 BERT FORMAT DEFINITIONS

Table 3-1 presents the T-Carrier BERT Format definitions that are unique to the Model 5500-700 Interface Module.

3.2 BER TEST ASSISTANCE

Table 3-2 presents a list of possible problem areas if the Model 5500 does not achieve synchronization with the device under test.

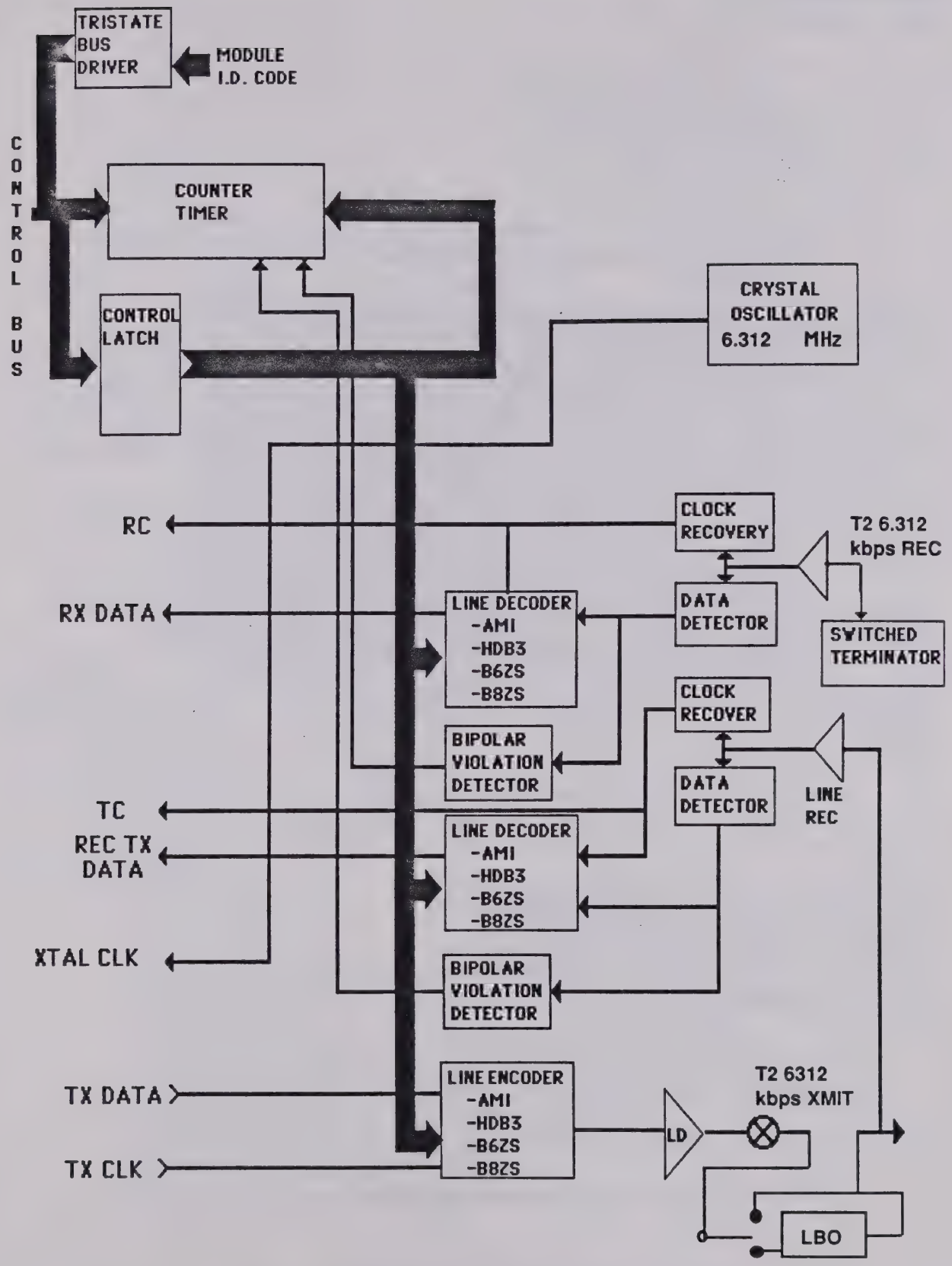


Figure 2-1. Model 5500-700 T-2 Interface Module Block Diagram

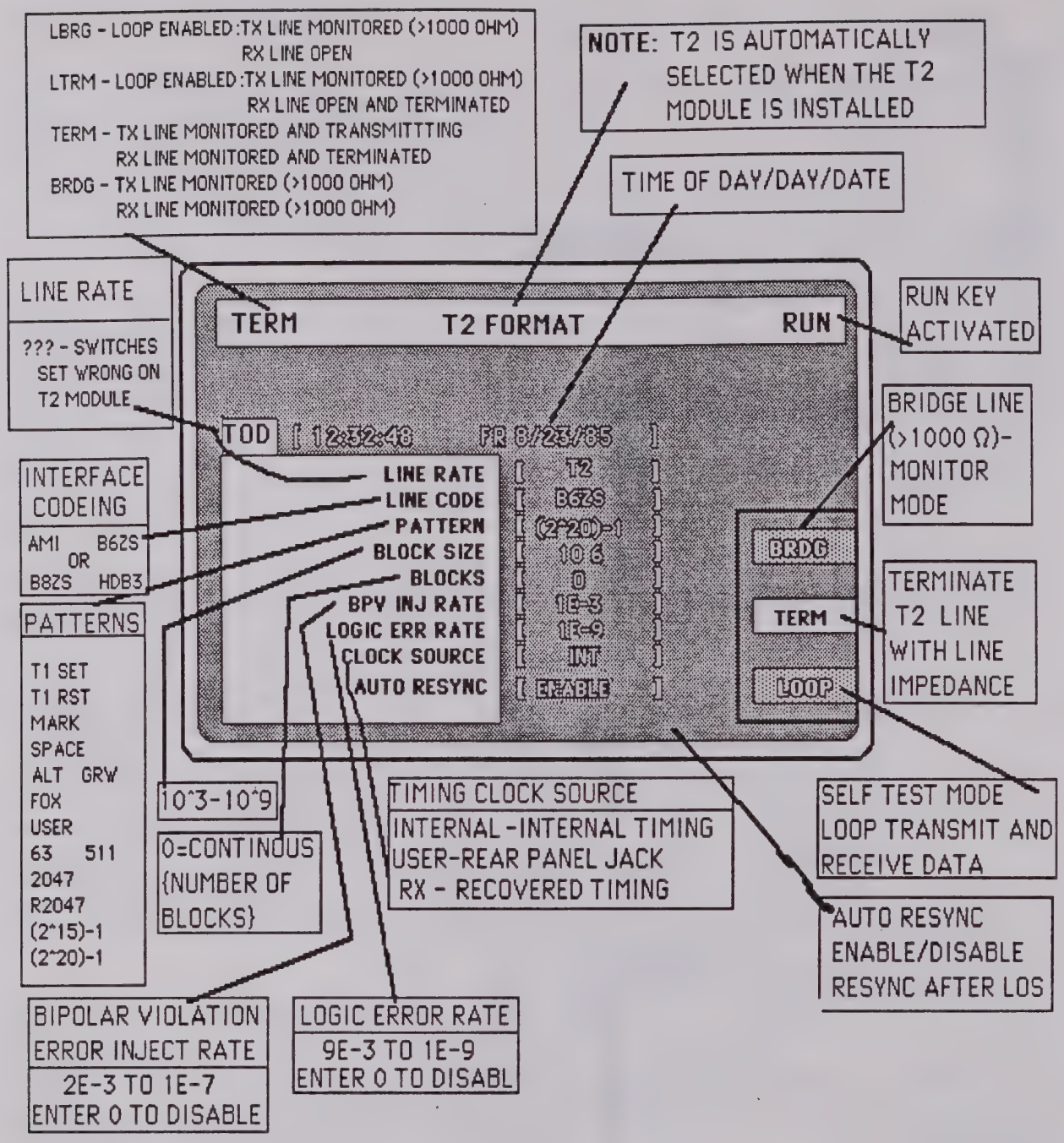


Figure 2-2. T-2 Format Menu

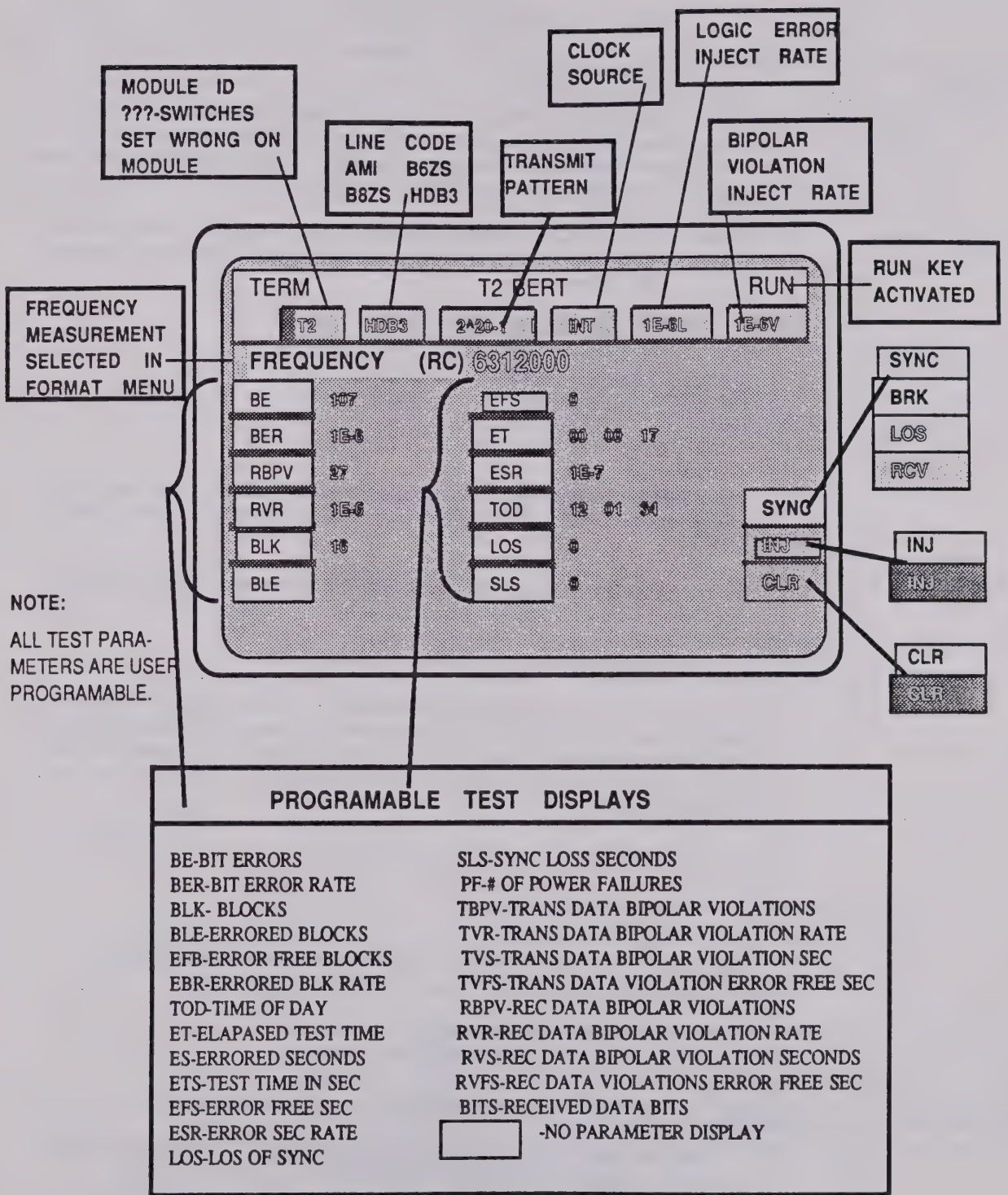


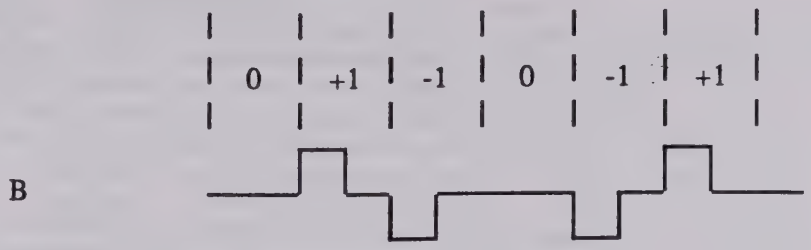
Figure 2-3. T-2 BERT Display

Table 3-1. BERT Format Definitions

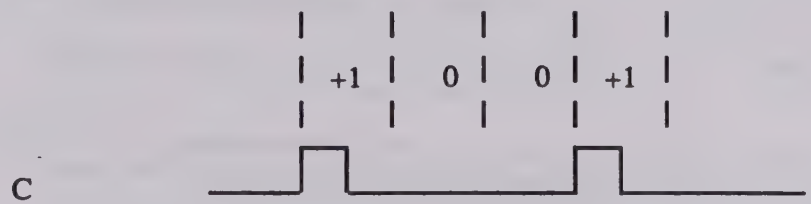
ITEM	DEFINITION
LINE RATE	This block displays the line rate as T1, T1C, or T2 for U.S. systems or 2.048 and 8.448 Mbps for CCITT G.703 modules. This is not a selectable parameter but is fixed by the interface module inserted into the Model 5500. It is a convenience item to remind the operator of the rate at which the Model 5500 is testing.
LINE CODE	The line code of the T-Carrier system under test may be selected by moving the half intensity block over the LINE CODE window and using the SELECT keys to choose the options. The options are: T1 AMI or B8ZS T1C AMI or B8ZS T2 AMI or B6ZS 2.048 Mbps AMI or HDB3 * 8.448 Mbps AMI or HDB3* * 2.048 Mbps and 8.448 Mbps G.703 modules are set for HDB3 at the factory and T-2 modules are set for B6ZS. A DIP switch on the module allows selection of AMI coding. The Alternate Mark Inversion (AMI) or Bipolar line code is the line code currently in use in the U.S. on all T1 baseband source code into AMI line code. Note that successive MARKS (1's) always alternate in polarity. A new format, Bipolar 8 Zero Substitution (B8ZS), is being considered for T1 in order to remove the restrictions on the number of successive SPACES (0's) which AMI places on the source coder. While not in actual use at the present time, this line code may become the future standard. An example of a B8ZS coded signal is provided in figure A. Assuming the last 1 transmitted was a positive "one". The polarities of the substituted word are simply reversed if the last "one was negative. 0 0 0 0 0 0 0 0 original word 0 0 0 +1 -1 0 -1 +1 substituted word BPV's always occur at the 4th and 7th bit positions of the substituted word. The line code used by T2 carrier systems is B6ZS which is similar to the B8ZS code previously discussed but which limits strings of 0's to less than 6. In this case a block of six consecutive zeros is substituted by the sequence "0 + - 0 - +" if the preceding mark was positive, or "0 - + 0 + -" if the preceding mark was negative (+ or - represents a positive or negative mark). An example of B6ZS coding is shown in figure B.

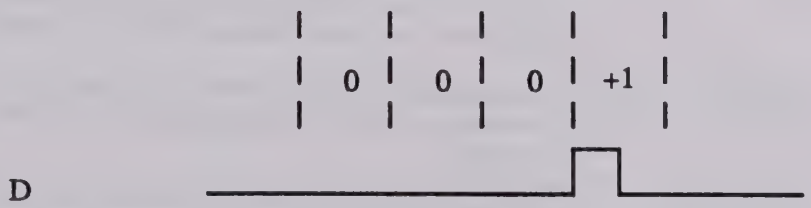
Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION



Finally, High Density, Bipolar 3 Zero Substitution (HDB3) line coding is used in European T-Carrier systems at 2.048 MBPS and 8.448 MBPS line rates. An example of this coding format is shown if figures C and D. (Preceding violation was negative and preceding pulse was negative in figure C and the preceding violation was negative and the preceding pulse was positve in figure D.)





The HDB3 coding process generates positive and negative marks alternately each time a binary logical 1 condition occurs within the message signal. However, unlike AMI coding, the maximum number of consecutive zeros is limited to a value of 3. If a series of 4 consecutive zeros does occur, the 4th zero is replaced by a mark referred to as a VIOLATION. The violation mark is always inserted with the same polarity as the preceding mark. This identifies the departure from the AMI scheme and indicates the occurrence of the violation.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
	In theory, if additional safeguards were not taken, it would be possible for several violations to have an identical polarity, and thus introduce a DC component into the signal. To overcome this problem, the coder continuously monitors the polarity of the last violation (may have been many bits earlier in the data stream) and the polarity of the last mark. The coder then forces the first bit of the 4-bit substitution sequence to a one or a zero, whichever is required, to allow the violation in the fourth bit position to be of opposite polarity to the previous violation.
PATTERN	The pattern choices from the regular FORMAT are all present in T-Carrier FORMAT, but the most useful patterns for T-Carrier testing are:
QRW QUASI-RANDOM WORD	A pattern of (2^20)-1 bits long which has built-in suppression of strings of 0's greater than 14. This pattern is the industry standard for T1 and T1C testing. (2^15)-1: A pseudo-random sequence used in European CCITT G.703 BER testing and jitter testing. (2^20)-1: A pseudo-random sequence of the same length as the QRW, but without the 14 zero suppression. Useful at T2 and for CCITT testing.
MARK	An all 1's pattern which may be used to simulate the "idle" pattern sent out by digital channel banks in an alarm condition.
USER	This is a user definable pattern of up to 135 characters (1080 bits) which could be used to send out patterns with more than 14 zeros or any other pattern a user may want to transmit.
T1 SET	This pattern sends out the standard T1 Channel Service Unit (CSU) loopback code (10000) to cause a remote CSU to loopback for test purposes. This code should be transmitted for 5 seconds before the CSU will loopback to prevent false loopbacks.
T1 RESET	This pattern sends out the standard T1 CSU reset code to return a CSU in loopback to normal operation. The code (100) should be sent out for 5 seconds to reset CSU loopback.
BPV INJ RATE	The user may select any rate of injection of Bipolar Violations from 2^{-3} to $1x^{-7}$ violation/bit. The rate is selected by changing the mantissa from 0 to 9 (a 0 disables the inject function) first and then moving the half intensity block to the right and changing the exponent from -3 to -7 as desired. The select keys or the HEX keypad can be used. A common rate is 1^{-3} which is useful in checking automatic protection switches. Pressing the INJ soft key on the main BERT display activates BPV Injection unless there is a "0" in the BPV in the inject rate mantissa.
LOGIC ERR RATE	Logic errors are what telephone companies call bit errors to distinguish them from BPV's. This rate of bit error injection is selectable from 9x10-3 to 1x10-9 errors/bit. The errors (and bipolar violations) are uniformly spaced throughout the bit stream when the INJ soft key is pressed. Note that the user is free to have either logic errors or BPV's or both injected.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
CLOCK SOURCE	The user may select from three alternatives depending upon what simulation is being attempted. When the Model 5500 is acting as the generator of the T- Carrier it is normal to choose INTERNAL timing so that the Model 5500 is the master clock. This would be the case whenever any loopback testing is performed. The "RX" or Receive Clock choice allows the user to operate a 5500 in what is called a loop timed mode. That is, the Model 5500 derives clock from the received bit stream and uses this to time its transmitter. This is useful if, for example, the user is making an end to end bit error test with Model 5500's at each end. In this case one of the test sets should be on INTERNAL (acting as the master clock) and the other should be set to RX. The final option available is USER which allows the operator to supply a TTL clock to the rear panel BNC connector. The clock supplied must be at the nominal bit rate of the module being used (i.e. 1.544 MHZ for T1 module, 6.312 MHZ for T2, etc..), and should be at least + 30ppm accurate.

Table 3-2. BER Test Assistance

SYMPTOM	POSSIBLE CAUSE
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Verify that BRIDGE mode in T- Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units.
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when test set stops. This is normal operation.
Model 5500 display errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. NOTE: T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.

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Model 5500-805

CCITT G.703 8.448 Mbps Interface Module

1.0 INTRODUCTION

The Model 5500-805 G.703 8448 Kbps Interface Module enables the Model 5500 to test data communication systems operating at G.703 8448 Kbps rates in accordance with the CCITT G.703 specification. The module provides the capability to transmit and receive data at the 8448 Kbps rate, in either HDB3 or AMI line code Formats, utilizing bipolar transmission techniques.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-805 Interface Module.

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-805 module enables the Model 5500 to generate and receive G.703 8448 Kbps serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consist of BNC type connectors for transmit and receive data, each with a separate grounding lug that enables the user to terminate the coaxial shield if desired, and a 15 pin subminiature D-type connector for transmit and receive data (used by some modem manufacturers) whose pins are in parallel with the transmit and receive BNC connectors.

The Generator section (refer to figure 2-1) consists of a line encoder, and a line driver. The line encoder can be configured to produce an AMI or HDB3 line code for the bit stream at the 8448 Kbps rate.

Table 2-1. Model 5500-805 Interface Module Specifications

CHARACTERISTIC	SPECIFICATION
TRANSMITTER	
Pulse Rate	8448 Kbps + 30 ppm
Output Pulse Amplitude	+2.37 v peak +10%
Output Pulse Shape	Rectangular
Overshoot	Less than 10% of amplitude height.
Line Code	HDB3 or AMI (User Selectable)
RECEIVER	
Input Impedance	75 ohms + 5% terminated. >1000 ohms bridged.
Input Level	+2.37 v peak plus up to 2000 ft. coaxial cable.

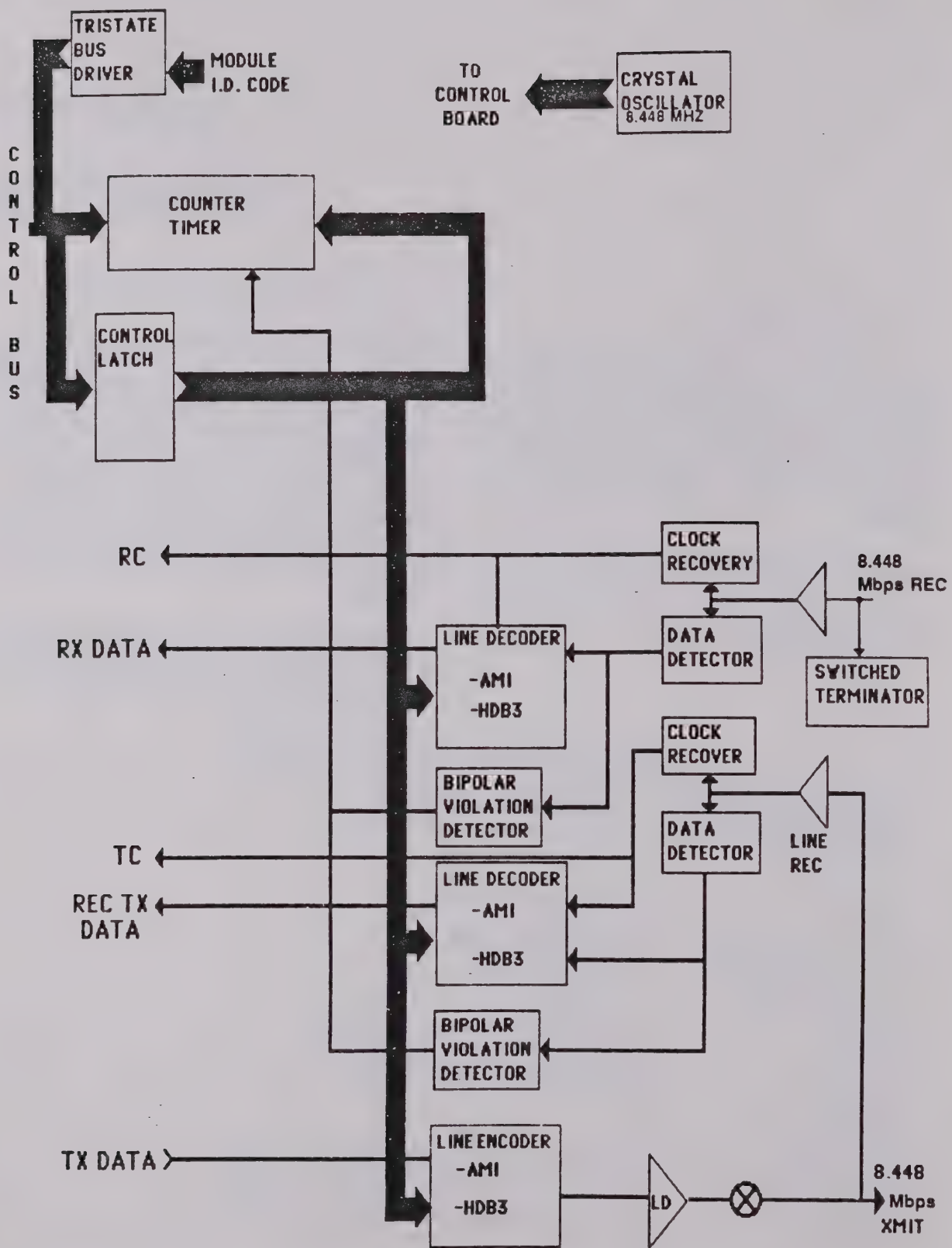
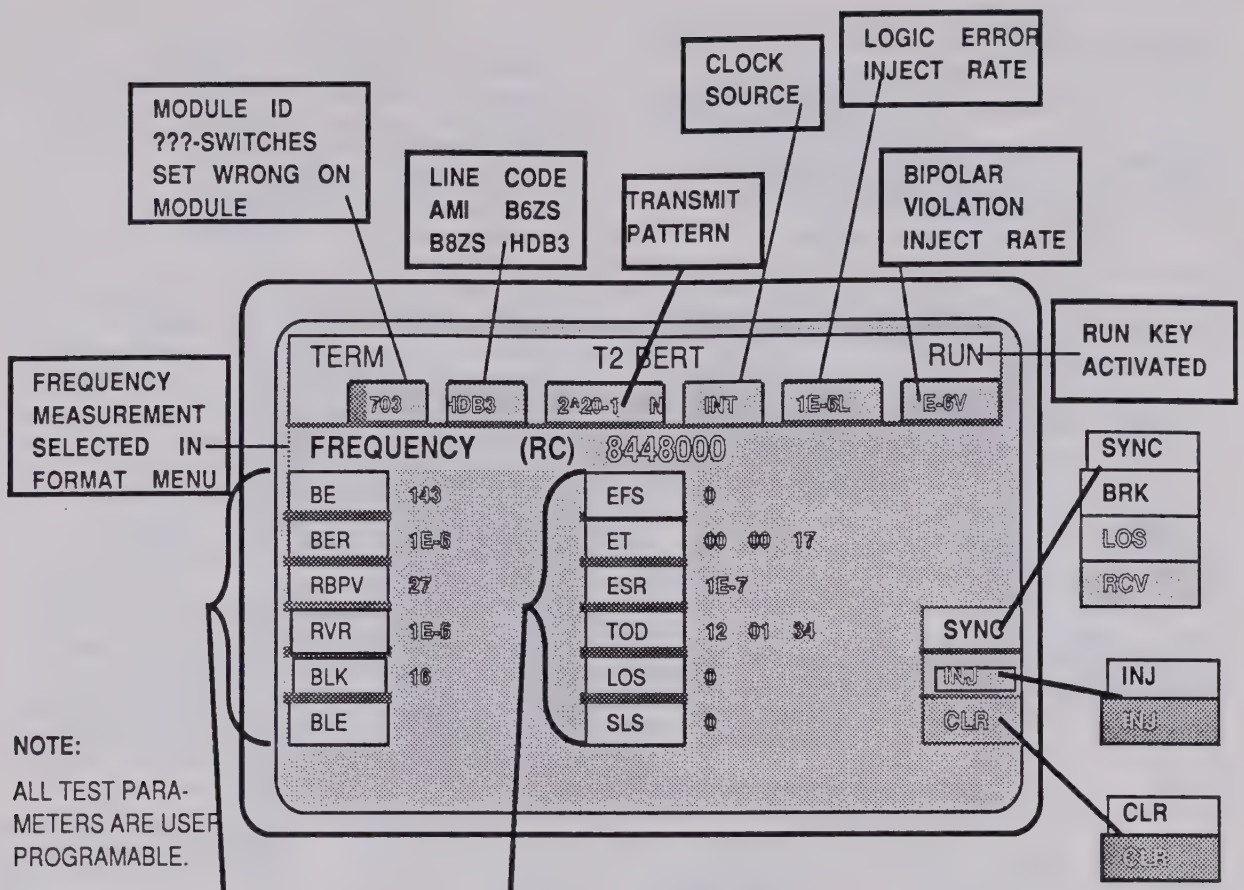


Figure 2-1. Model 5500-805 Interface Module Block Diagram



PROGRAMABLE TEST DISPLAYS

BE-BIT ERRORS
BER-BIT ERROR RATE
BLK- BLOCKS
BLE-ERRORED BLOCKS
EFB-ERROR FREE BLOCKS
EBR-ERRORED BLK RATE
TOD-TIME OF DAY
ET-ELAPASED TEST TIME
ES-ERRORED SECONDS
ETS-TEST TIME IN SEC
EFS-ERROR FREE SEC
ESR-ERROR SEC RATE
LOS-LOS OF SYNC
SLS-SYNC LOSS SECONDS
PF-# OF POWER FAILURES
TBPV-TRANS DATA BIPOLAR VIOLATIONS
TVR-TRANS DATA BIPOLAR VIOLATION RATE
TVS-TRANS DATA BIPOLAR VIOLATION SEC
TVFS-TRANS DATA VIOLATION ERROR FREE SEC
RBPV-REC DATA BIPOLAR VIOLATIONS
RVR-REC DATA BIPOLAR VIOLATION RATE
RVS-REC DATA BIPOLAR VIOLATION SECONDS
RVFS-REC DATA VIOLATIONS ERROR FREE SEC
BITS-RECEIVED DATA BITS
-NO PARAMETER DISPLAY

Figure 3-1. Model 5500-805 BERT Display

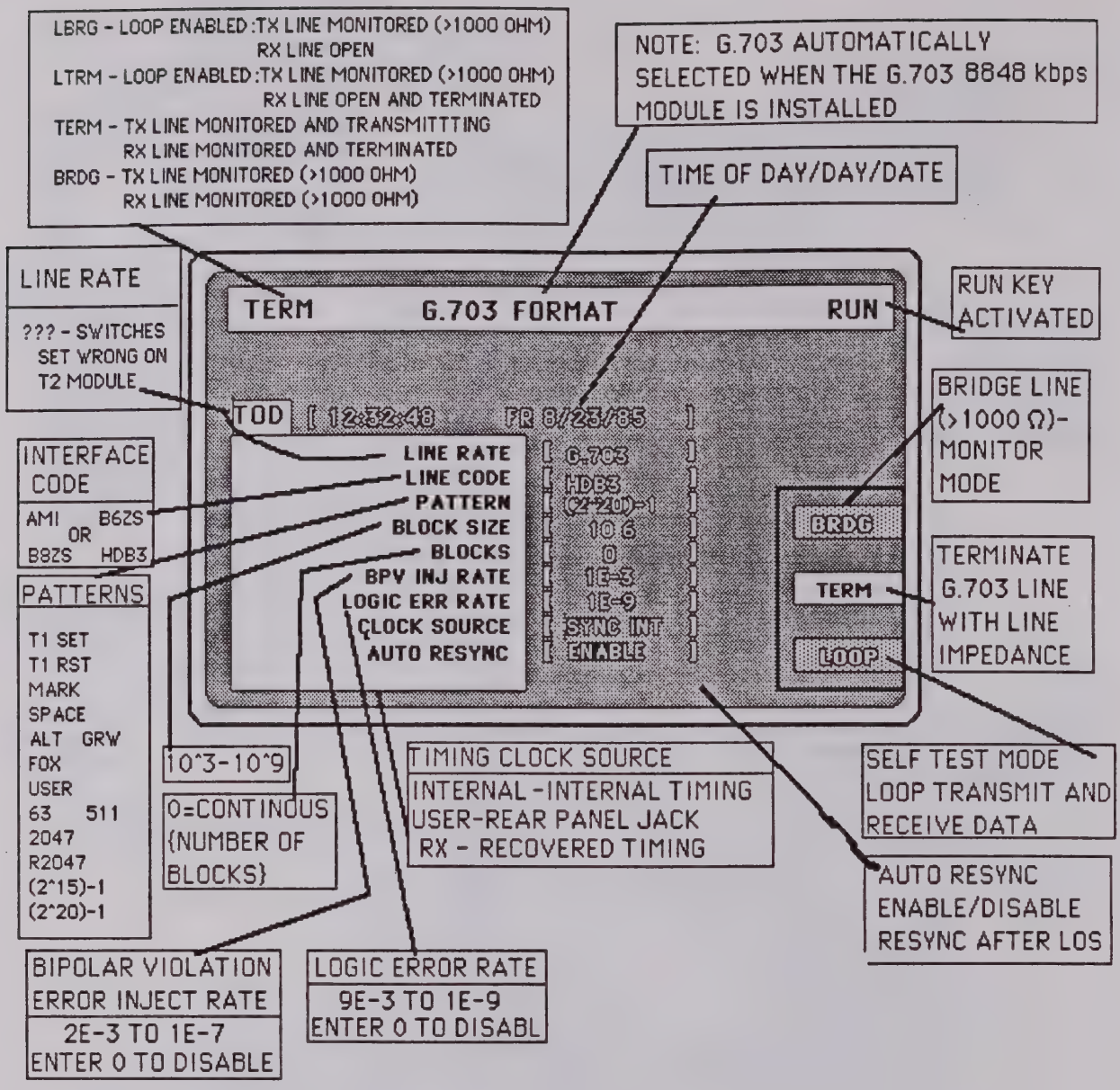


Figure 3-2. Model 5500-805 BERT Format

The receive section of the module contains two independent receivers. This configuration enables the Model 5500 to monitor both receive pair and Transmit pair traffic for Bipolar Violations. The Receive input has a switchable line termination to enable it to receive input signals and terminate them in 75 ohms, as well as monitor signals in a Bridged mode. With the exception of the switchable impedance each receiver is the same. The receiver section recovers and regenerates the signal at the cross connect point. The clock recovery circuit (basically a phase locked loop) derives timing from the incoming bit stream and feeds it to the data detector, line decoder, and Model 5500 internal logic. The Receive Clock and received Transmit Clock are both recovered in this manner.

The Data Detector accepts the output signal of the Receiver and combines it with the recovered clock to do the final reshaping and regeneration of the input which is then passed to the Line Decoder and Bipolar Violation Detector. The Line Decoder is set to AMI or as appropriate and converts the line coded signal to a TTL level bit stream for analysis by the Model 5500 internal logic. The BPV detector compares the output of the Data Detector to the AMI coding rule and passes information on violations of the rule to both the line Decoder and Counter Timer circuits which in turn initiate the count of BPV's displayed on the CRT.

3.0 OPERATION

The Model 5500 G.703 BERT Display and Format Menus (refer to figures 3-1 and 3-2) contain an area that displays the line code. When position 1, SW3, of the G.703 8448 Kbps Interface Module is in the "ON" position, these display areas will display "B6ZS" or "HDB3". When the switch is in the "OFF" position, these display areas will display "AMI" or "B8ZS". Since G.703 8448 Kbps will only utilize AMI or HDB3, the proper line code may be selected via the menu soft keys once the switch on the G.703 8448 Kbps Interface module has been placed in the desired position.

In the HDB3 mode of operation the Line Decoder and Bipolar Violation Detector combine to ignore intentional Bipolar Violations.

3.1 LINE MODE SELECTION

Selection of the desired line mode is performed in the following manner:

1) Remove the top cover of the G.703 8448 Kbps Interface Module, held in place with four Phillips head screws.

2) Carefully separate the top PC board (G.703 8448 Kbps I/O Module Board) from the bottom PC board (G.703 8448 Kbps Control Board) and remove the transmit and receive cable connectors from the top PC board.

3) Configure SW3, position 1, for the desired line code (refer to figure 3-3). Select "ON" for HDB3 or "OFF" for AMI.

4) Reassemble the module, taking care not to bend any of the pins on the connectors between the top and bottom PC boards.

NOTE: Positions of switches other than SW 3, position 1, are shown for illustration **ONLY**, and may or may not reflect the switch positions set at the factory for your card.

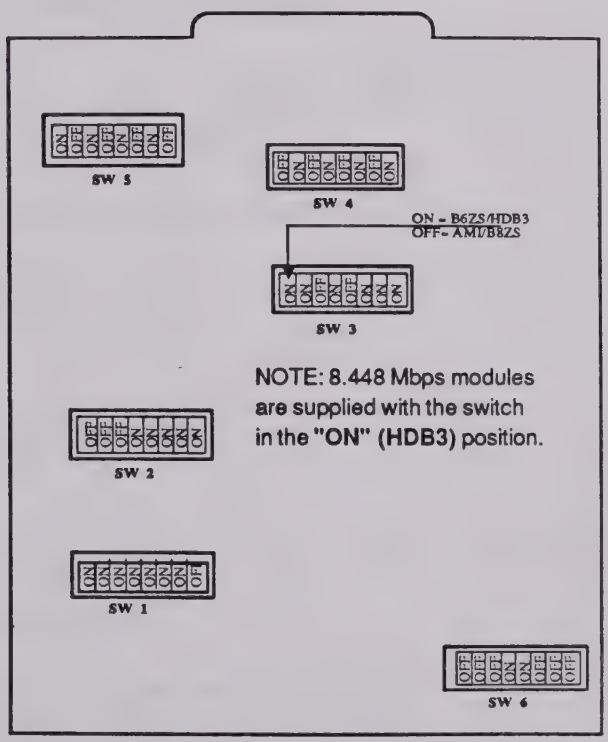


Figure 3-3. G.703 8448 Kbps Line Code Selection

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Model 5500-810 G.703 64KBPS Interface Module

1.0 INTRODUCTION

The model 5500-810 G.703 64 KBPS Interface Module enables the model 5500 to test digital transmission systems operating at the 64 Kbps rate in accordance with CCITT recommendation G.703. The module enables the 5500 to transmit and receive data and clock signals in any of the three modes of operation specified in CCITT recommendation G.703; codirectional interface mode, centralized clock interface mode, and both the line side and service side of the contradirectional interface mode. In addition the model 5500, when equipped with the 5500-810 interface module, has the capability to provide Octet timing, injection and detection of bipolar violations, clock error detection, codirectional code violation detection, byte synchronous user pattern transmission, high impedance monitoring of live traffic in the receive direction, low level and high level transmission, and internal loop back.

The mechanical interface between the 5500-810 interface module and the system under test consists of four Western Electric Company type 310 compatible jacks for transmit and receive data and clock. A 25 pin D type connector is wired in parallel with the type 310 jacks.

2.0 DESCRIPTION

2.1 SPECIFICATIONS

Tables 2-1 through 2-4 present the specifications for the model 5500-810 G.703 Interface Module.

Table 2-1. Model 5500-810 Codirectional Mode Specifications.

CHARACTERISTIC	SPECIFICATION
Transmitter - TX Data	
Data Rate	64 KBPS (256 Kbaud codirectional encoding)
Pulse Shape	Retangular
Pulse Amplitude	±1.0 volt ±10% into 120 ohms
Pulse Width	3.9us ±10% at 50% amplitude
Line Code	In accordance with codirectional conversion rules. Binary "1" encoded as 1100; binary "0" encoded as 1010. Polarity alternates every successive four bit code providing a bipolar transmission consisting of four-bit blocks

Table 2-1. Model 5500-810 Codirectional Mode Specifications (Cont).

CHARACTERISTIC	SPECIFICATION
Timing	User selectable 8kHz timing provided by violating the alternation in polarity every 8th block.
Receiver - RX Data	
Input Impedance	115 ohms ±5% terminated. Greater than 1000 ohms in high impedance monitor mode.
Input Level	1.0 volt peak plus up to 3db attenuation at 128 kHz

Table 2-2. Model 5500-810 Centralized Clock Mode Specifications

CHARACTERISTIC	SPECIFICATION
Transmitter - TX Data	
Data Rate	64 KBPS derived from TX CLK input
Pulse Shape	Retangular
Pulse Amplitude	User Selectable into 110 ohms Low level 1.0 volt ± .1 volt High level 3.0 volts ± .5 volt
Pulse Width	15.6 us ±10% at 50 percent amplitude derived from TX CLK input.
Line Code	Bipolar Alternate Mark Inversion
Rise and Fall Times	Less than 1 usec
Receiver - RX Data	
Input Impedance	115 ohms ±5% terminated >1000 ohms in high impedance monitor mode
Input Level	Low Level = 1.0 volt ± 0.1 volt plus up to 450 meters of interconnecting twisted pair cable. High Level = 3.0 volts ± 0.5 volt plus up to 450 meters of interconnecting cable.

Table 2-2. Model 5500-810 Centralized Clock Mode Specifications (Cont).

CHARACTERISTIC	SPECIFICATION
Receivers - TX CLK RX CLK	
Input Impedance	115 ohms ±5% terminated >1000 ohms in high impedance monitor mode
Input Level	Low Level = 1.0 volt ± 0.1 volt plus up to 450 meters of interconnecting twisted pair cable.
	High Level = 3.0 volts ± 0.5 volt plus up to 450 meters of interconnecting cable.
Pulse Width	a) 7.8 us - 50% duty cycle b) 9.8 - 10.9 us - 63 - 70% duty cycle
Line Code	Bipolar Alternate Mark Inversion Receiver will support octet timing (8kHz) produced by violating the polarity of every 8th clock pulse.

Table 2-3. Model 5500-810 Contradirectional Mode (Line Side) Specifications.

CHARACTERISTIC	SPECIFICATION
Transmitter - TX Data	
Data Rate	64 KBPS
Pulse Shape	Rectangular
Pulse Amplitude	1.0 volt ±10% into 120 ohms
Pulse Width	15.6 us ±10% at 50 percent amplitude
Line Code	Bipolar Alternate Mark Inversion
Transmitter - TX CLK RX CLK	
Clock Rate	64 kHz
Pulse Shape	Rectangular
Pulse Amplitude	1.0 volt ±10% at 50 percent amplitude

Table 2-3. Model 5500-810 Contradirectional Mode (Line Side) Specifications (Cont).

CHARACTERISTIC	SPECIFICATION
Pulse Width	7.8 us ±10% at 50% amplitude
Line Code	Bipolar Alternate Mark Inversion Transmitters support user selectable octet timing by violating the clock pulse polarity every 8th clock pulse. Leading edge of clock pulse corresponds to leading edge of data bit.
Receiver - RX Data	
Input Impedance	115 ohms ±5% terminated. >1000 ohms in high impedance monitor mode
Input Level	1.0 volt ±10% plus up to 3db attenuation at 32 kHz

Table 2-4. Model 5500-810 Contradirectional Mode (Service Side) Specifications.

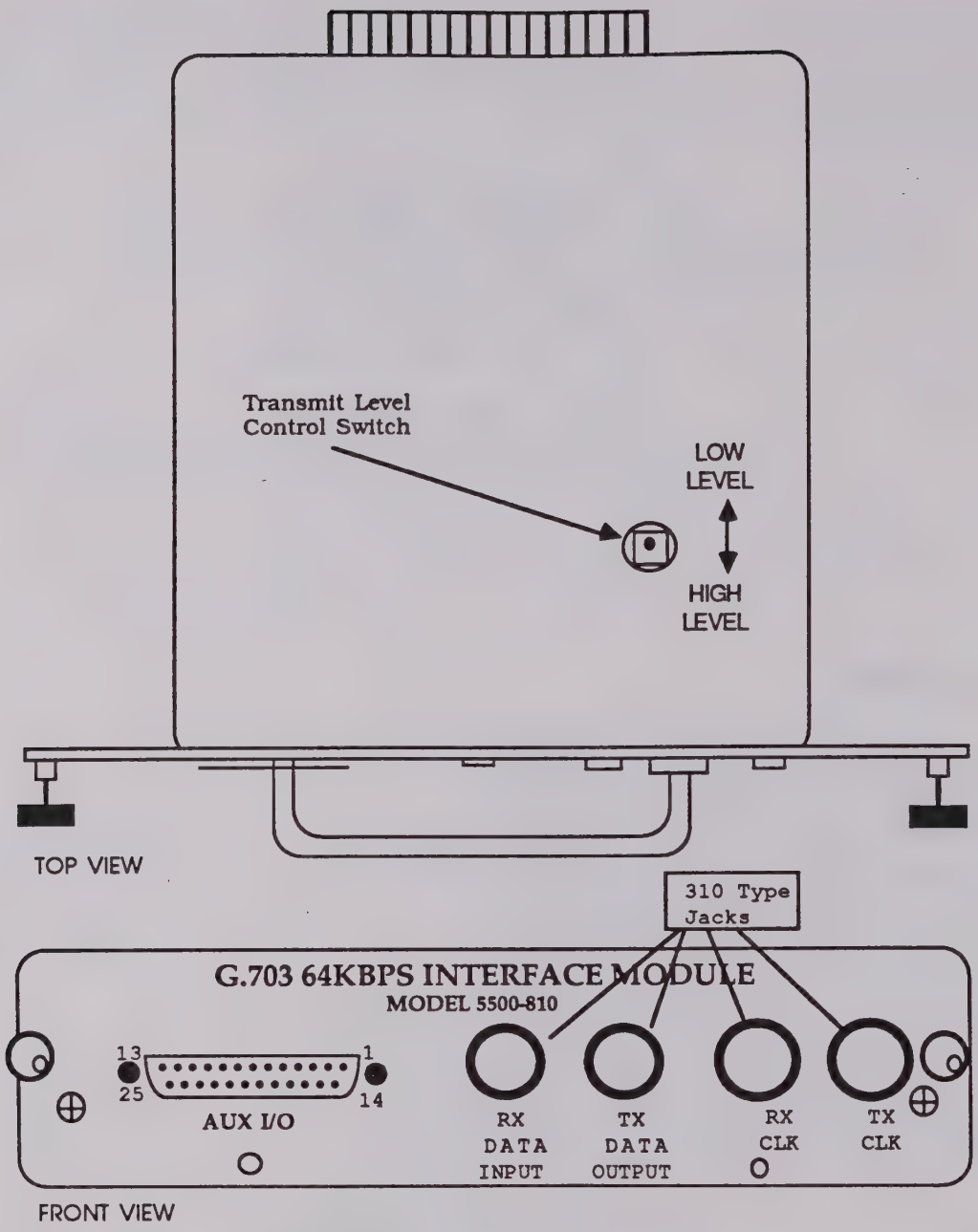
CHARACTERISTIC	SPECIFICATION
Transmitter - TX Data	
Data Rate	64 KBPS derived from TX CLK input
Pulse Shape	Rectangular
Pulse Amplitude	1.0 volt ±10% into 120 ohms
Pulse Width	15.6 us ±10% at 50 percent amplitude derived from TX CLK input
Line Code	Bipolar Alternate Mark Inversion
Receiver - RX Data	
Input Impedance	115 ohms ±5% terminated. Greater than 1000 ohms in high impedance monitor mode.
Input Level	1.0 volt peak ±10% plus up to 3db attenuation at 32kHz

Table 2-4. Model 5500-810 Contradirectional Mode (Service Side) Specifications (Cont).

CHARACTERISTIC	SPECIFICATION
Receivers - TX CLK RX CLK	
Input Impedance	115 ohms ±5% terminated >1000 ohms in high impedance monitor mode
Input Level	1.0 volt peak ±10% plus up to 3db attenuation at 64kHz
Pulse Width	a) 7.8 us ±10% at 50% amplitude
Line Code	Bipolar Alternate Mark Inversion Receivers will support octet timing (8kHz) produced by violating the polarity of every 8th clock pulse.

2.2 DIAGRAMS

Figure 2-1 presents the outline drawing of the 5500-810 interface module showing the location of the level select switch. Figure 2-2 illustrates the 5500-810 BERT format menu while figures 2-3 and 2-4 represent the codirectional BERT menu and contradirectional Bert menu respectively. Figure 2-5 is a simplified block diagram of the three modes of operation available with the 5500-810 while figure 2-6 is a timing diagram of those modes of operation. Figure 2-7 is an overall block diagram of the model 5500-810 interface module.



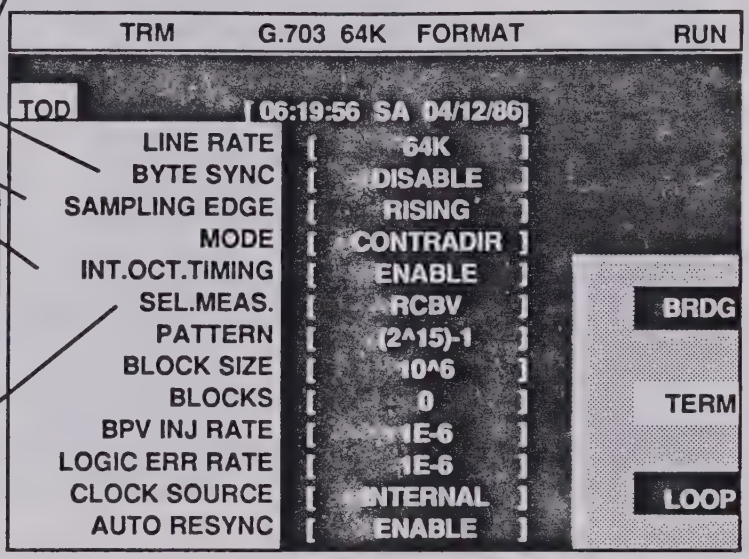
AUX I/O PINOUT

1 - TX SHIELD	14 - TX RTN
2 - TX	15 - RX SHIELD
3 - RX	16 - RX RTN
4 - TX CLK SHIELD	17 - TX CLK RTN
5 - TX CLK	18 - RX CLK SHIELD
6 - RX CLK	19 - RX CLK RTN
7 THRU 13 - NOT USED	20 THRU 25 - NOT USED

Model 5500-810 Outline Drawing
Figure 2-1

SAMPLING EDGE RISING/FALLING Selects which receive clock edge will be used to sample receive data in the contradirectional mode. Disabled in the codirectional mode.

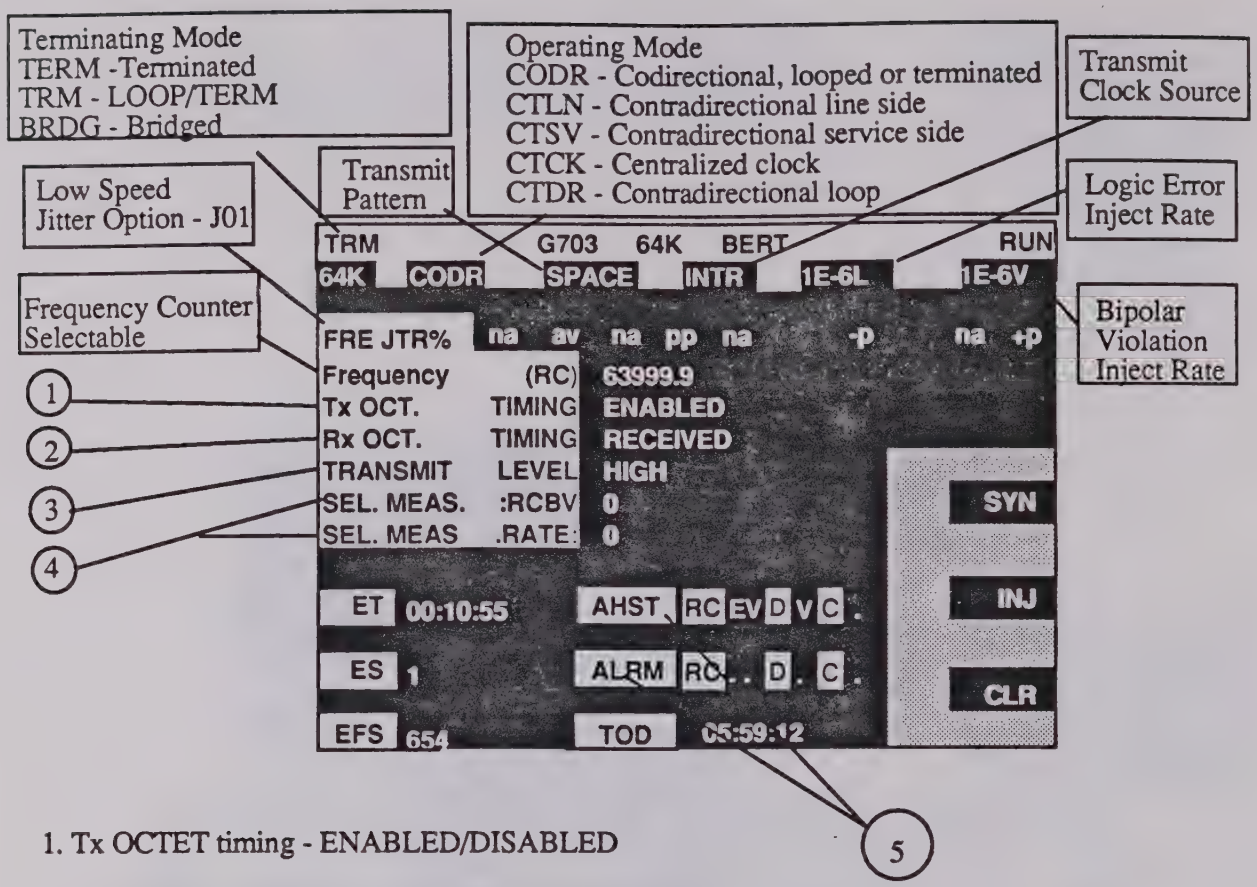
BYTE SYNC - ENABLE/DISABLE - Selects byte synchronous transmission of user pattern



INT. OCT. TIMING ENABLE/DISABLE Controls OCTET timing of the transmit clock and data

SEL. MEAS. - Selects the parameter to be measured by the module. (See BERT menu)

Model 5500-810 BERT Format Menu
Figure 2-2



1. Tx OCTET timing - ENABLED/DISABLED

2. Rx OCTET timing - RECEIVED/NOT RECEIVED

3. Transmit Level - Peak level of transmit data and clock
   Controlled by switch on module High=3V peak, Low=1V peak

4. SEL. MEAS.:RCBV - Parameter that has been selected for measurement by the module

   RCBE - Received clock bit error (missing or extra pulse) - extracted from Rx data
   RCBV - Received clock bipolar violation - extracted from Rx data
   RDCV - Received data coding violations (4-bit encoding violation)
   RDBV - Received data bipolar violations that are not OCTET violations. Also includes missing OCTET violations.

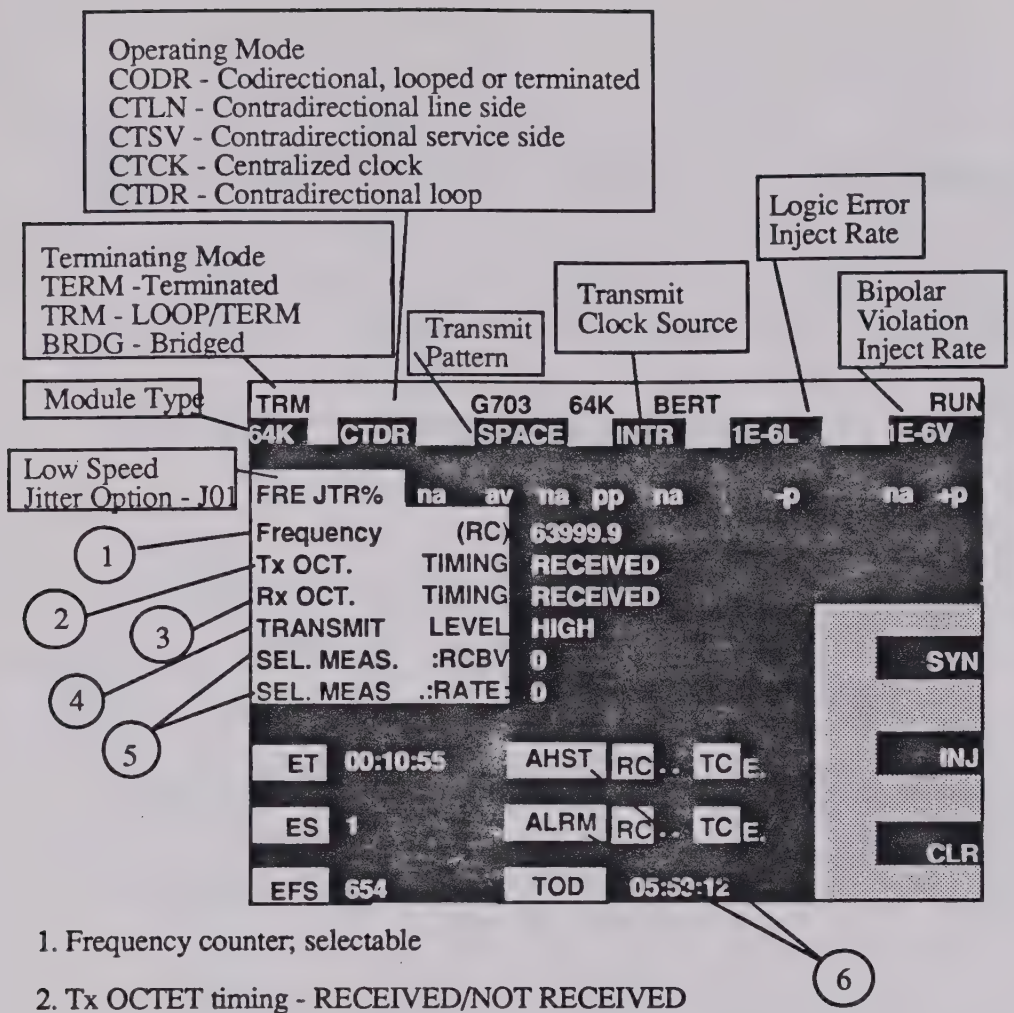
   SEL. MEAS.:RATE - Total number of bits divided by SEL. MEAS. count

5. ALRM RC .. D . C . - Displays occurance of clock bit errors (E), clock bipolar violations (V), Data bipolar violations (V), and data 4-bit coding violations (V).

   AHST RC . . D . C . - Displays history of clock bit errors (E), clock bipolar violations (V), Data bipolar violations (V), and data 4-bit coding violations (V) if either occurs during test.

   RCBE RCBV RDBV RDCV (Same for ALRM - "." indicates no occurance)

Model 5500-810 Codirectional Mode BERT Menu
Figure 2-3



1. Frequency counter; selectable

2. Tx OCTET timing - RECEIVED/NOT RECEIVED

3. Rx OCTET timing - RECEIVED/NOT RECEIVED

4. Transmit Level - Peak level of transmit data and clock
   Controlled by switch on module High=3V peak, Low=1V peak

5. SEL. MEAS.:RCBV - Parameter that has been selected for measurement by the module

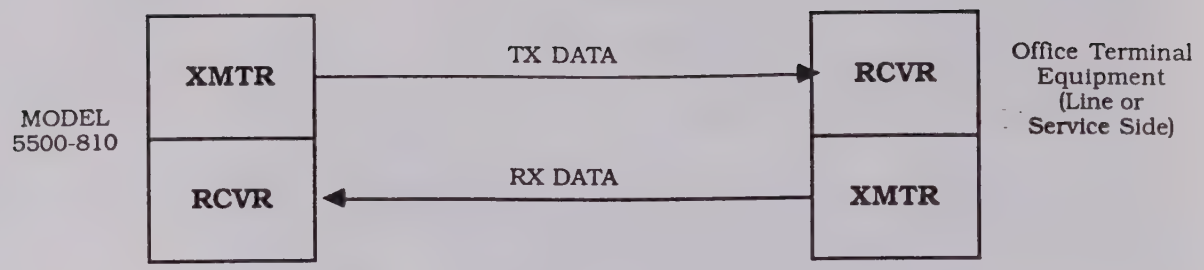
   RCBE - Received clock bit error (missing or extra pulse)
   RCBV - Received clock bipolar violation
   TCBE - Transmit clock bit errors
   TCBV - Transmit clock bipolar violations

   SEL. MEAS.:RATE - Total number of bits divided by SEL. MEAS. count

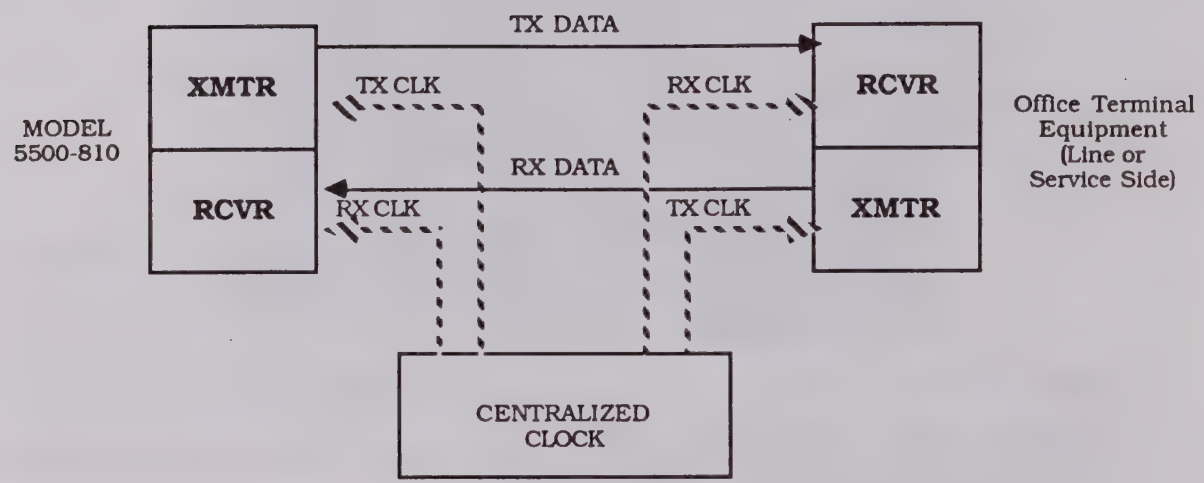
6. ALRM RC .. TC .. -Displays occurances of clock bit errors (E) or bipolar violations (V)
   "." indicates no occurance

   AHST RC .. TC .. - Displays history of clock bit errors (E) or bipolar violations (V)
   if either occurs during test. "." indicates no occurance

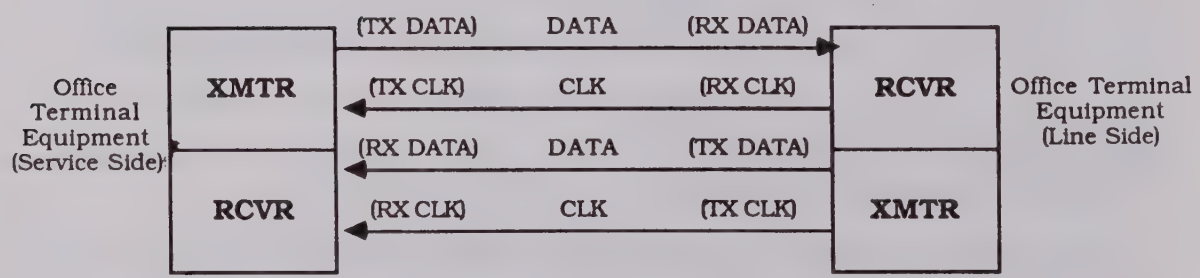
Model 5500-810 Contradirectional Mode BERT Menu
Figure 2-4



CODIRECTIONAL MODE



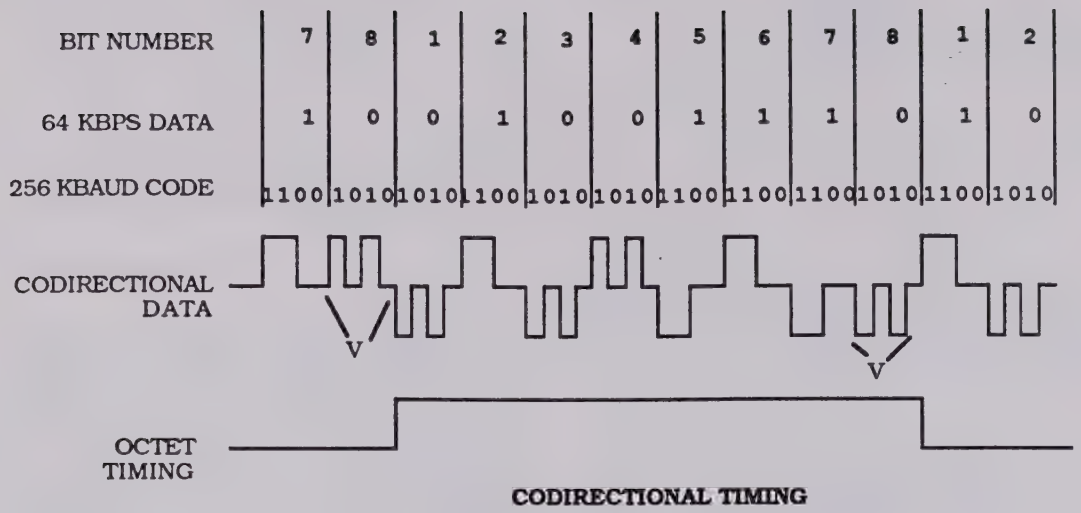
CENTRALIZED CLOCK MODE



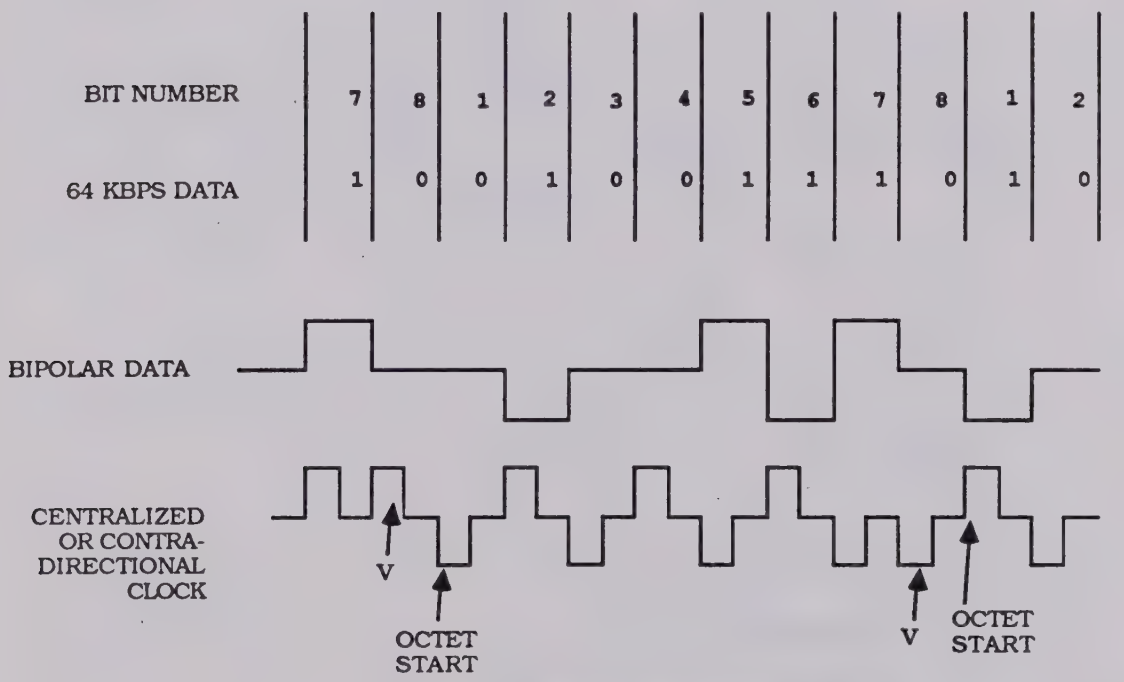
Model 5500-810 can simulate either line or service side

CONTRADIRECTIONAL MODE

Model 5500-810 Mode Block Diagrams
Figure 2-5

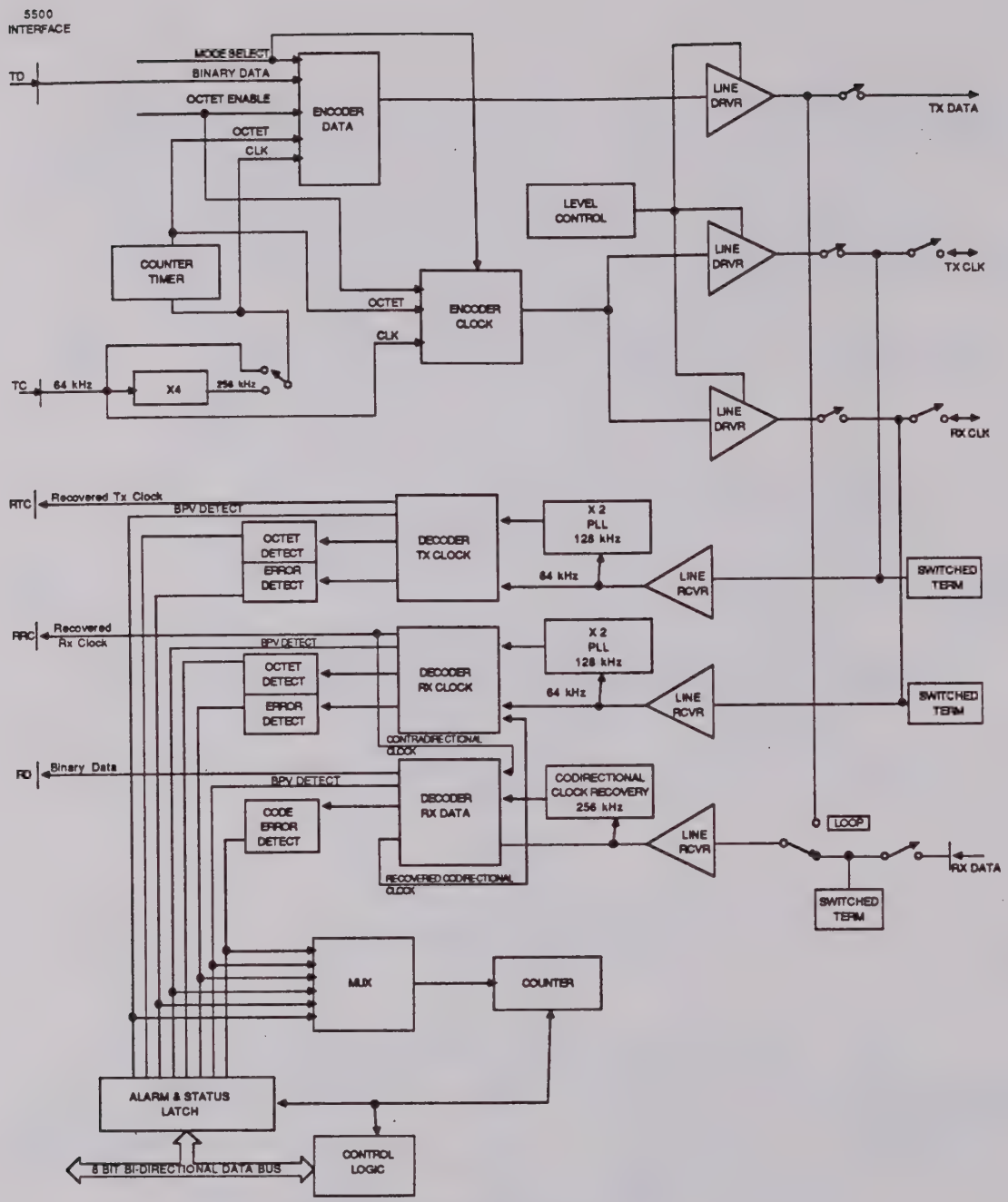


CODIRECTIONAL TIMING


BIT NUMBER
7 8 1 2 3 4 5 6 7 8 1 2
64 KBPS DATA
1 0 0 1 0 0 1 1 1 0 1 0
BIPOLAR DATA
CENTRALIZED OR CONTRA-DIRECTIONAL CLOCK
V
OCTET START
V
OCTET START

CENTRALIZED CLOCK TIMING AND CONTRADIRECTIONAL TIMING

Model 5500-810 Mode Timing Diagrams
Figure 2-6



Model 5500-810 Interface Module Block Diagram
Figure 2-7

Model 5500-815

G.703 2.048 MBPS Interface Module

1.0 INTRODUCTION

The model 5500-815 G.703 2.048 MBPS Interface Module enables the model 5500 to test data communications systems operating at the 2.048 MBPS data rate in accordance with CCITT recommendation G.703. The module allows the model 5500 to transmit and receive 2.048 MBPS data, inject and detect bit errors and bipolar violations on pre-selected data patterns, inject bipolar violations and bit errors in live traffic, and operate as a transparent regenerative repeater. With the addition of the model 5500-J05 high speed jitter option (see model 5500-J05 option), the model 5500-815 will enable the model 5500 to perform high speed jitter analysis with pre-selected data patterns and inject or remove high speed jitter from live traffic. The line code format, AMI or HDB3, for transmit and receive data is user selectable.

The mechanical interface between the model 5500-815 and the system under test consists of two BNC coaxial connectors for transmit and receive data, 2 corresponding binding posts for terminating the coaxial shield of each transmission line if desired, and two BNC coaxial connectors for use with the high speed jitter option; one to inject a signal to modulate transmitted jitter and the other to detect the demodulated receive jitter.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the model 5500-815 2.048 MBPS interface module.

Table 2-1. Model 5500-815 Interface Module Specifications

CHARACTERISTIC	SPECIFICATION
Pulse Rate	2.048 MBPS ±50PPM
Line Code	User Selectable AMI or HDB3
Transmit Pulse Amplitude	2.37V ±10% into a 75 ohm load
Nominal Pulse Width	244 ns ±10% at 50% amplitude
Receiver Input	2.37 volt peak plus up to 4000 feet coaxial cable
Input Impedance	75 ohms

2.1 FUNCTIONAL DESCRIPTION

The model 5500-815 G.703 2.048 MBPS module block diagram is presented in figure 2-1. The module consists of four basic functional areas; the transmitter, receiver, retransmitter/repeater, and control logic.

The transmitter section consists of a TX clock select multiplexer, an AMI/HDB3 line encoder, a bait error/bipolar violation injector, and a line driver. The clock selector can multiplex any one of four choices for the transmit clock including a jittered clock or an average (de-jittered) clock, with the 5500-J05 option installed. The AMI/HDB3 line encoder formats the transmitted data into user selectable AMI or HDB3 bipolar line code. CCITT recommendation G.703 specifies HDB3 for encoding the 2.048 MBPS data rate, however, AMI line coding is available for user specific applications. The bit error/bipolar violation injector can be used to inject bit errors and/or bipolar violations in the transmitted data stream. In the normal mode (retransmit disabled) bit errors are injected into the binary data internal to the 5500, before encoding, such that the alternate mark inversion polarity of the line is reversed as shown in figure 2-2. In the retransmit mode bit errors are injected into the bipolar waveform in such a way as to simulate a noise spike or anomaly on the transmit pair that would suppress a "1" (mark) such that it would appear as a "0" (space) or to inject a "1" in a manner that it would appear as a noise spike where a "0" would normally occur as illustrated in figure 2-3. This mode also creates a bipolar violation since the alternate mark inversion scheme has been disturbed without changing the overall line polarity with respect to error free data. Bipolar violations may also be injected in either mode without creating bit errors. In the normal mode, the user has the option of injecting bit errors only, bipolar violations only, or both simultaneously. The injection rates for bit errors and/or bipolar violations are independent in the normal mode. In the retransmit mode, the user has the choice of injecting bipolar violations only or both bit errors and the corresponding bipolar violations simultaneously. Since there is one bipolar violation for each bit error injected in the retransmit mode, the error injection rates will be the same. Following data encoding, a line driver is employed to convert the bipolar data to the appropriate 2.37 volt peak transmit level.

The receiver input consists of a 75 ohm switched line terminater that permits the receiver to terminate a line or to operate in a high impedance bridged monitor mode. **BRDG** must be selected on the format menu to operate in the high impedance mode. An ALBO (automatic line build-out) clock recovery and data detector circuit provides the necessary data reconstruction and clock recovery to convert the bipolar waveform into TTL levels for analysis. A line decoder converts the AMI or HDB3 line code formats to binary data and a bipolar violation detector and counter detects bipolar violations that are not part of the HDB3 line encoding. Decoded binary data and clock are then presented to the model 5500 for bit error analysis.

The retransmitter/repeater consists of a FIFO (first in-first out) register that converts the receive data rate to a user selectable rate for retransmissions. The user may select a retransmit clock from the following choices:

RX CLK - RECEIVE CLOCK (NORMAL REPEATER)

JIT CLK - JITTERED RX CLOCK (INJECT JITTER INTO LIVE TRAFFIC)*

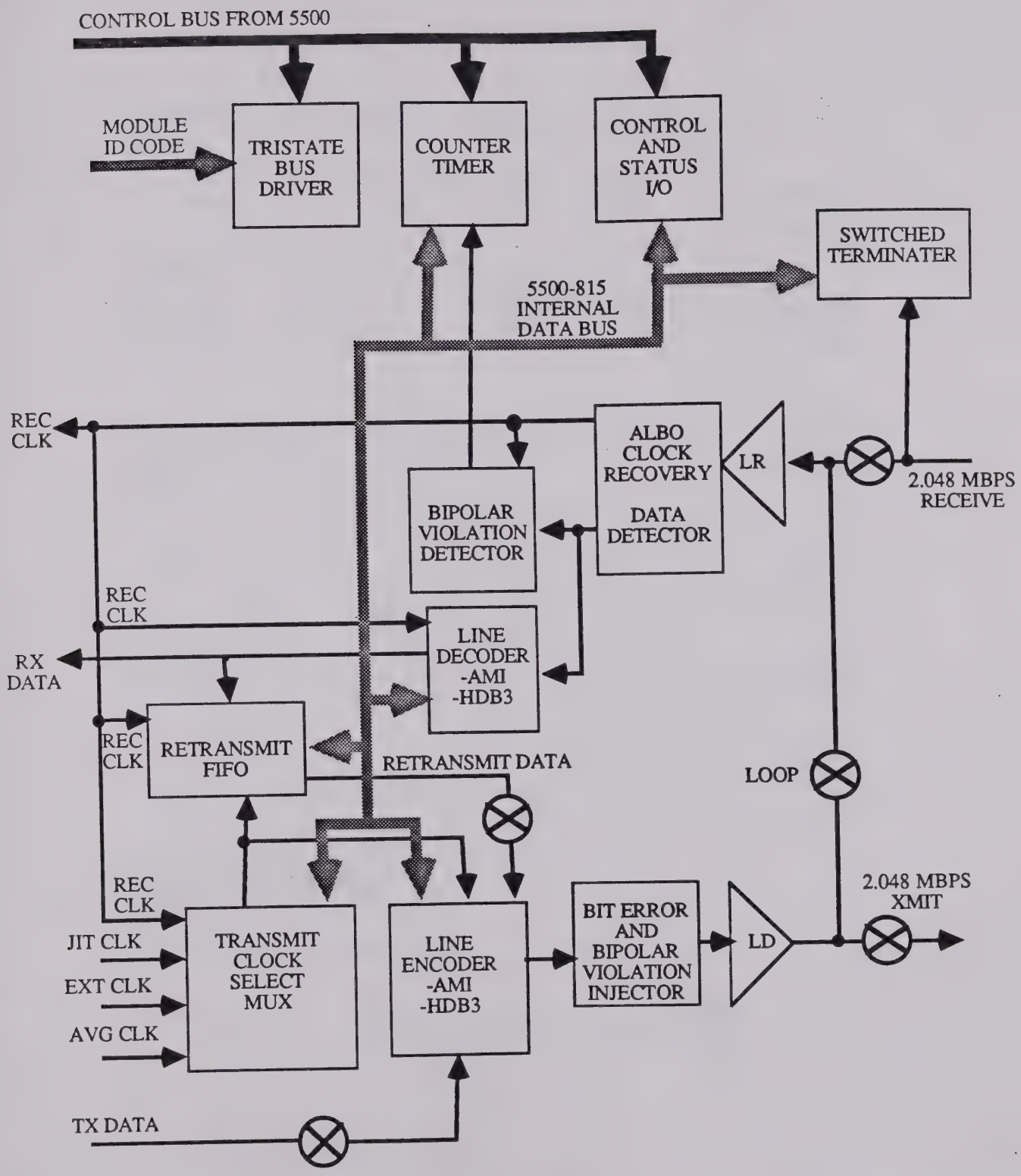
AVG CLK - AVERAGED RX CLOCK (REMOVE JITTER FROM LIVE TRAFFIC)*

*Available with model 5500-J05 option only.

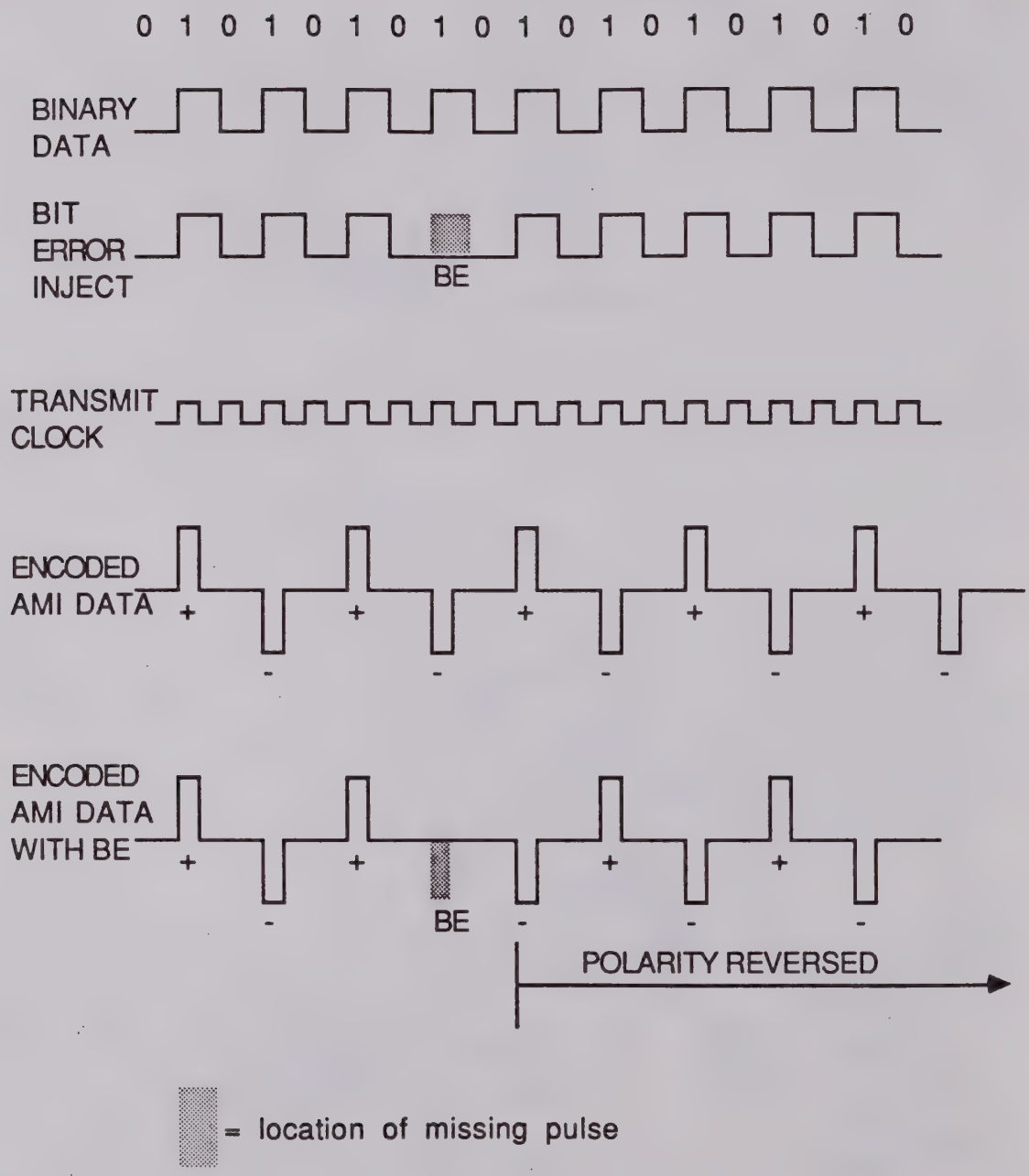
All functions of the model 5500-815 are controlled via a bank of status and control latches. These latches are controlled by the model 5500 via an 8-bit control bus.

3.0 OPERATION

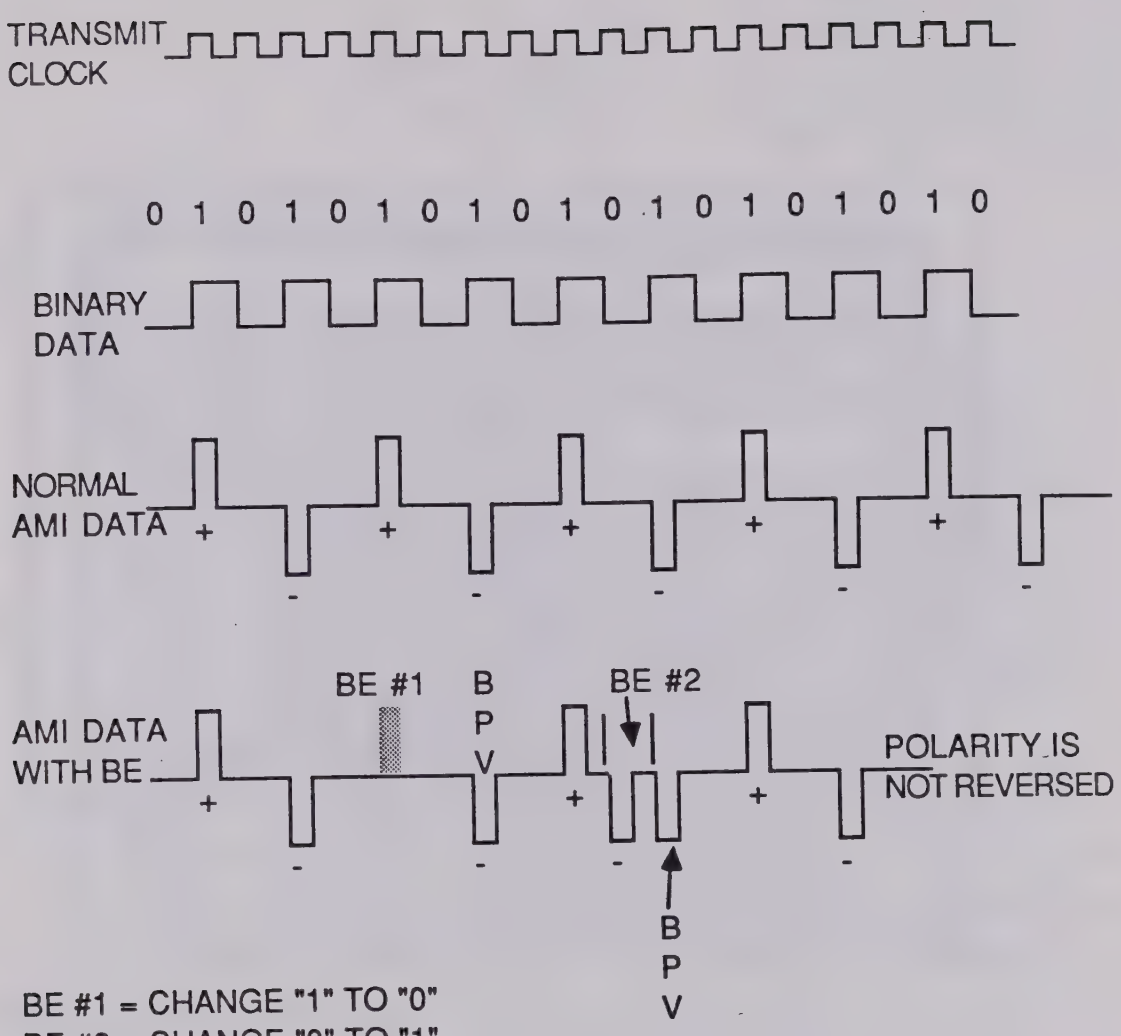
Figures 3-1 and 3-2 illustrate the model 5500-815 format menus while figures 3-3 and 3-4 present the 5500-815 BERT menus.



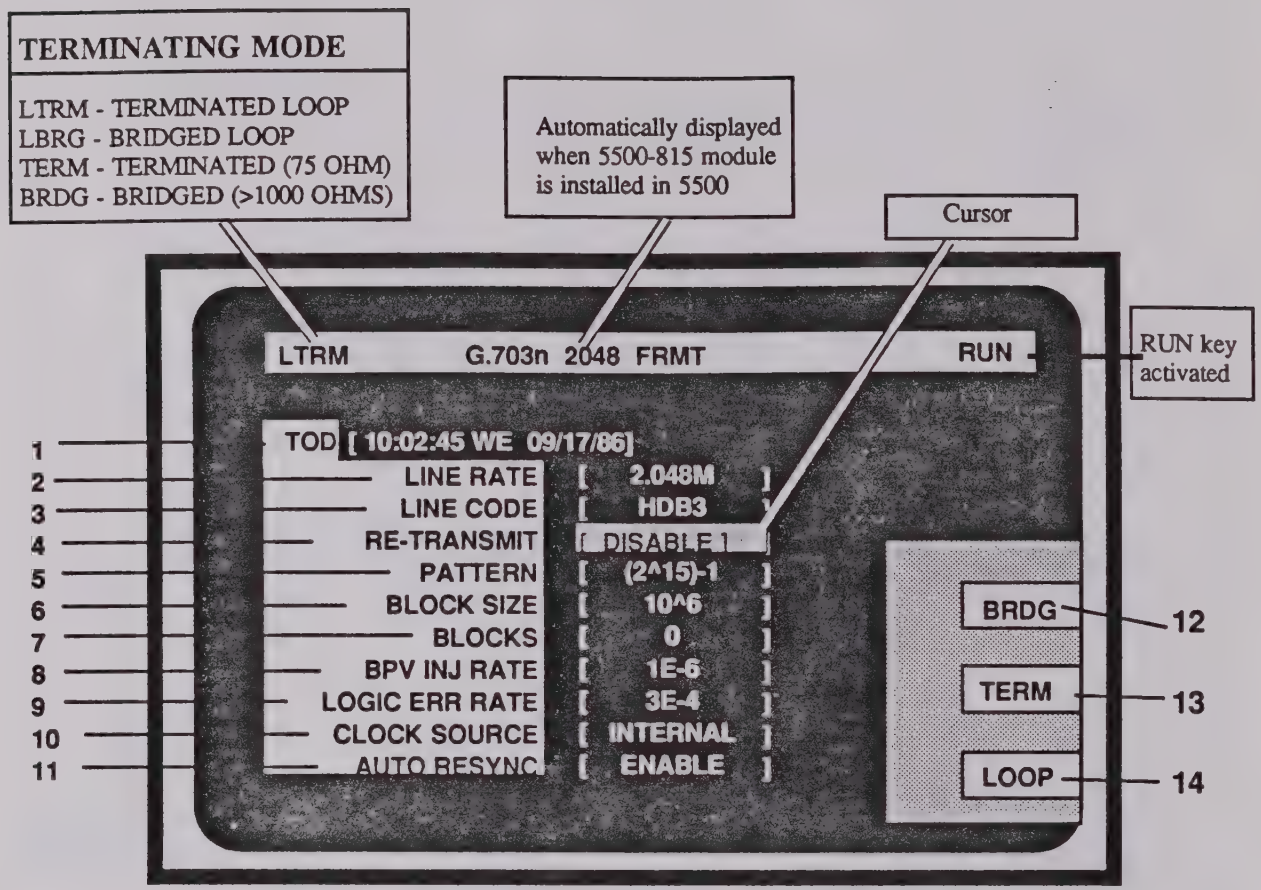
Model 5500-815 Interface Module Block Diagram
Figure 2-1



Normal Bit Error Injection
Figure 2-2


TRANSMIT CLOCK
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
BINARY DATA
NORMAL AMI DATA
+
-
AMI DATA WITH BE
BE #1
B P V
BE #2
POLARITY IS NOT REVERSED
B P V
BE #1 = CHANGE "1" TO "0"
BE #2 = CHANGE "0" TO "1"
= location of missing pulse

Retransmit Bit Error Injection
Figure 2-3



Line 1. TOD = Time of Day/Day/Date

Line 2. LINE RATE = G.703 2.048 MBPS

Line 3. LINE CODE = Selectable AMI or HDB3

Line 4. RE-TRANSMIT = Enabled or Disabled

Line 5. PATTERN = Transmit pattern

Line 6. BLOCK SIZE = Selectable 10^3 to 10^9

Line 7. BLOCKS = 0 is continuous

Line 8. BPV INJ RATE = Bipolar violation inject rate

Line 9. LOGIC ERR RATE = Bit error inject rate

Line 10. CLOCK SOURCE = Transmit clock source; Internal clock, user clock, RX-receive clock,J05-jitter clock

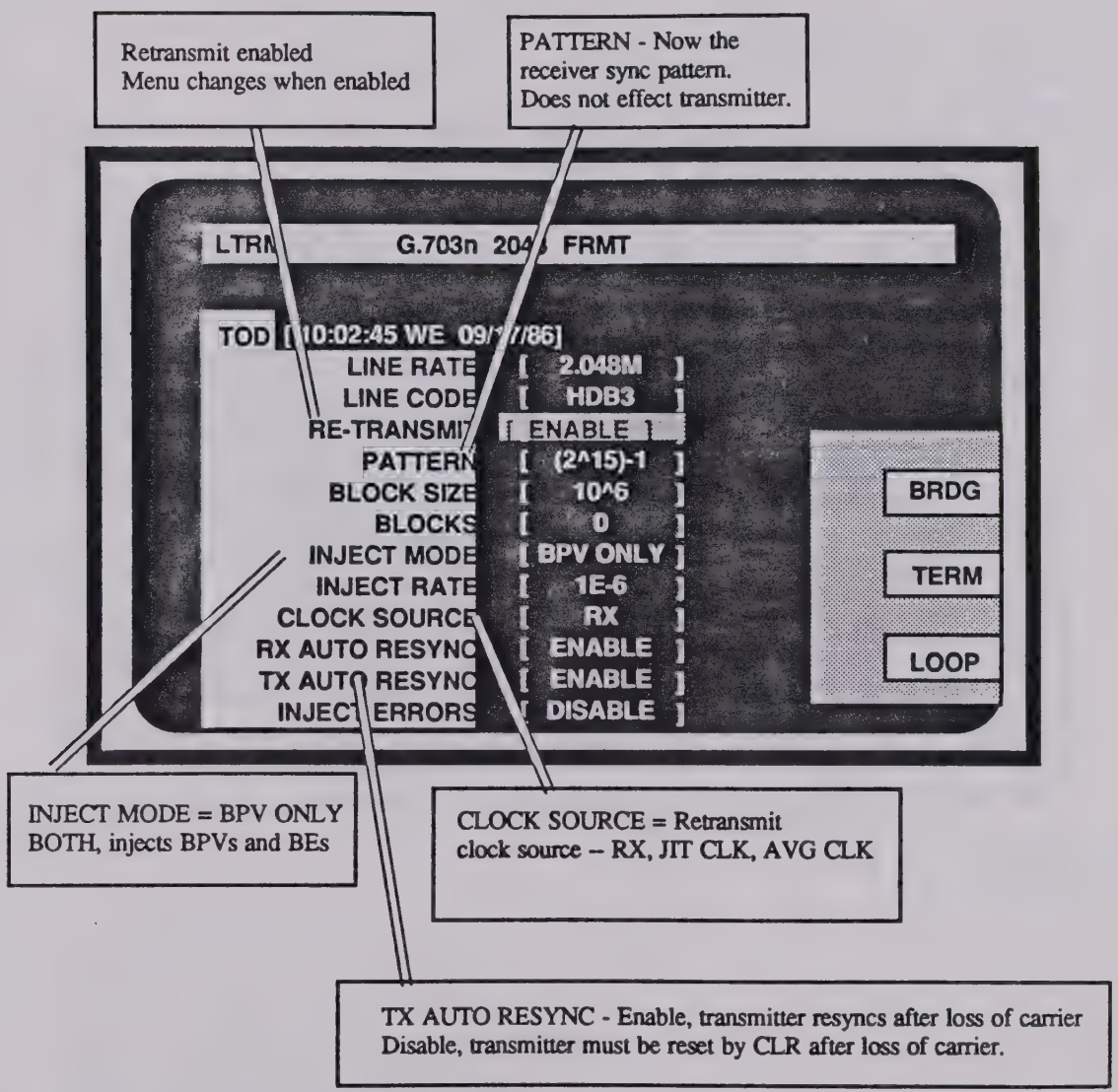
Line 11. AUTO RESYNC = Enabled/Disabled = When enabled receiver will resync when burst errors exceed 100 BE/sec -- Disabled, receiver will not attempt to resync in the presence of burst errors

Line 12. BRDG = Bridged mode, RX input >1000 ohms--TX output open

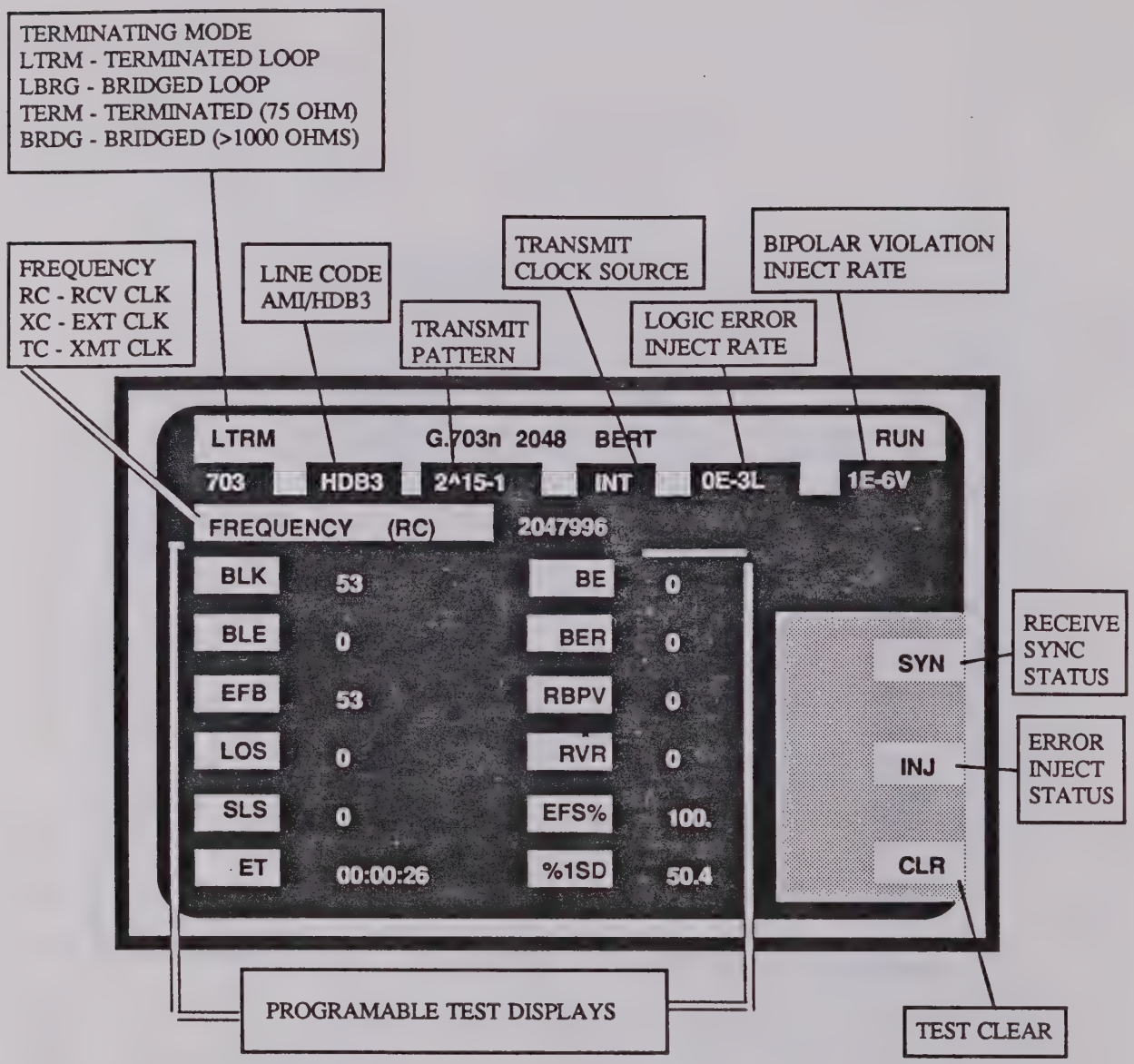
Line 13. TERM = Terminate mode, both RX and TX terminated in 75 ohms

Line 14. LOOP = Internal loop back self test mode

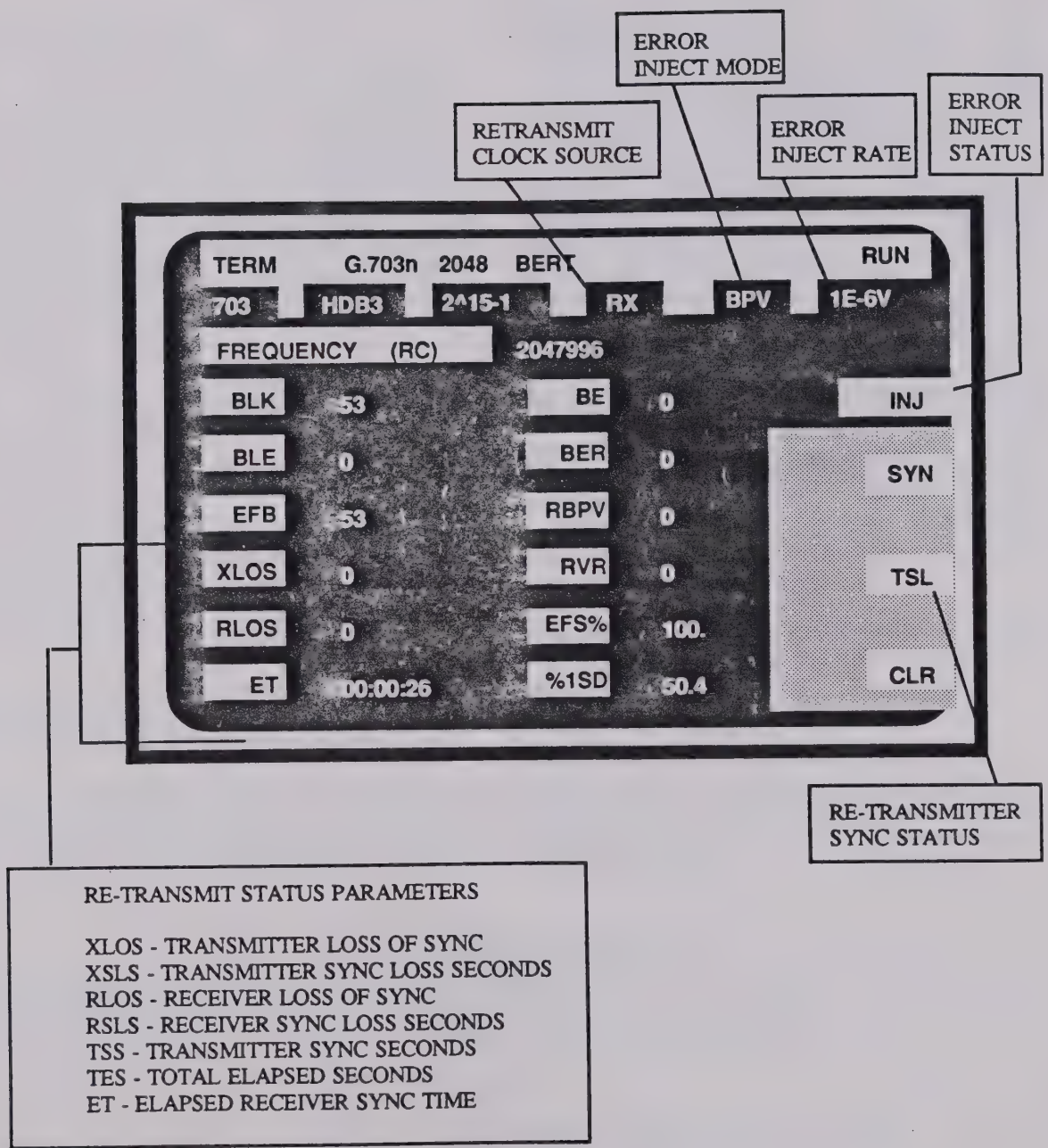
5500-815 Format Menu - Normal Mode
Figure 3-1


Retransmit enabled
Menu changes when enabled
PATTERN - Now the
receiver sync pattern.
Does not effect transmitter.
LTRM G.703n 204 FRMT
TOD [10:02:45 WE 09/ /86]
LINE RATE [2.048M]
LINE CODE [HDB3]
RE-TRANSMI [ENABLE]
PATTERN [(2^15)-1]
BLOCK SIZE [10^6]
BLOCKS [0]
INJECT MODE [BPV ONLY]
INJECT RATE [1E-6]
CLOCK SOURCE [RX]
RX AUTO RESYNC [ENABLE]
TX AUTO RESYNC [ENABLE]
INJECT ERRORS [DISABLE]
BRDG
TERM
LOOP
INJECT MODE = BPV ONLY
BOTH, injects BPVs and BEs
CLOCK SOURCE = Retransmit
clock source -- RX, JIT CLK, AVG CLK
TX AUTO RESYNC - Enable, transmitter resyncs after loss of carrier
Disable, transmitter must be reset by CLR after loss of carrier.

5500-815 Format Menu - Retransmit Mode
Figure 3-2



5500-815 BERT Menu - Normal Mode
Figure 3-3



5500-815 BERT Menu - Retransmit Mode
Figure 3-4

NOTE

When injecting bipolar violations only, with HDB3 line encoding selected, and transmitting a pseudo random pattern, a situation can occur where the randomly injected BPV occurs in the data stream at a point that will cause the three preceding bits of the data stream and the bipolar violations to appear as HDB3 substitution code for a stream of four consecutive zeros. This phenomenon will occassionally result in the bipolar violation not being detected since it appears to be part of the HDB3 code substitution and at least one but not more than four bit errors. There is a probability of this phenomenon occurring whenever bipolar violations are injected into a HDB# encoded bit stream that can contain at least two consecutive zeros. It is suggested that bipolar violation injection testing be done only with the MARK or ALT pattern or a USER pattern that does not contain two or more consecutive zeros when operating with HDB3 line code. In user specific applications where data is inverted before transmission (logic "1" transmitted as space, etc.), it is suggested that BPV injection testing be done only with the **SPACE** or **ALT** pattern or a **USER** pattern that does not contain two or more consecutive ones. Unless otherwise specified, units are shipped from the factory configured to invert data before transmission.

Model 5500-J01

Low Speed Jitter Option

1.0 INTRODUCTION

The Model 5500-J01 option enables the user to measure low speed (75 to 72000 bps) jitter and read the results on the main BERT display. The J01 option consists of a printed circuit card which is mounted in the bottom of the 5500 chassis. Control, status, and data interface signals are connected to the 5500 control board via a 34 pin ribbon cable. Power, consisting of +5 VDC and ground, is received thru the board on a 2 pin connector cabled to the main power supply.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-J01 low speed jitter option.

2.1 FUNTIONAL DESCRIPTION

The 5500-J01 option uses a sampling technique to measure edge timing difference on the received data. The received data is sampled at approximately 250 times the bit rate. The result of this sample is used to synchronize an internal clock to the average data transitions.

Edge jitter is then calculated by measuring the percent of difference between the actual transitions of the received data and the transitions of the synchronized internal clock.

It should be noted that this sampling technique depends on transitions to acheive accuracy and synchronize the internal clock. Therefore, long periods of one's (1's) or zero's (0's) may result in inaccurate readings.

3.0 OPERATION

The 5500-J01 option permits the display of measured jitter results as four different readings (all as a percent of bit period) on the main BERT display (refer to figure 3-1). These readings will continually vary if the FRE mode has been selected or will be presented as a peak hold reading in the HLD mode. When the HLD mode is selected, the reading displayed will be the largest reading obtained after depressing the CLR switch to begin the test.

The four readings are:

pp Represents peak-to-peak or the largest differences in edges during 1024 samples at frequencies above 300 bps or 256 samples below 300 bps.

+p Represents the largest difference in data edges that is later than the internal oscillator.

-p Represents the largest difference in data edges that is earlier than the internal oscillator.

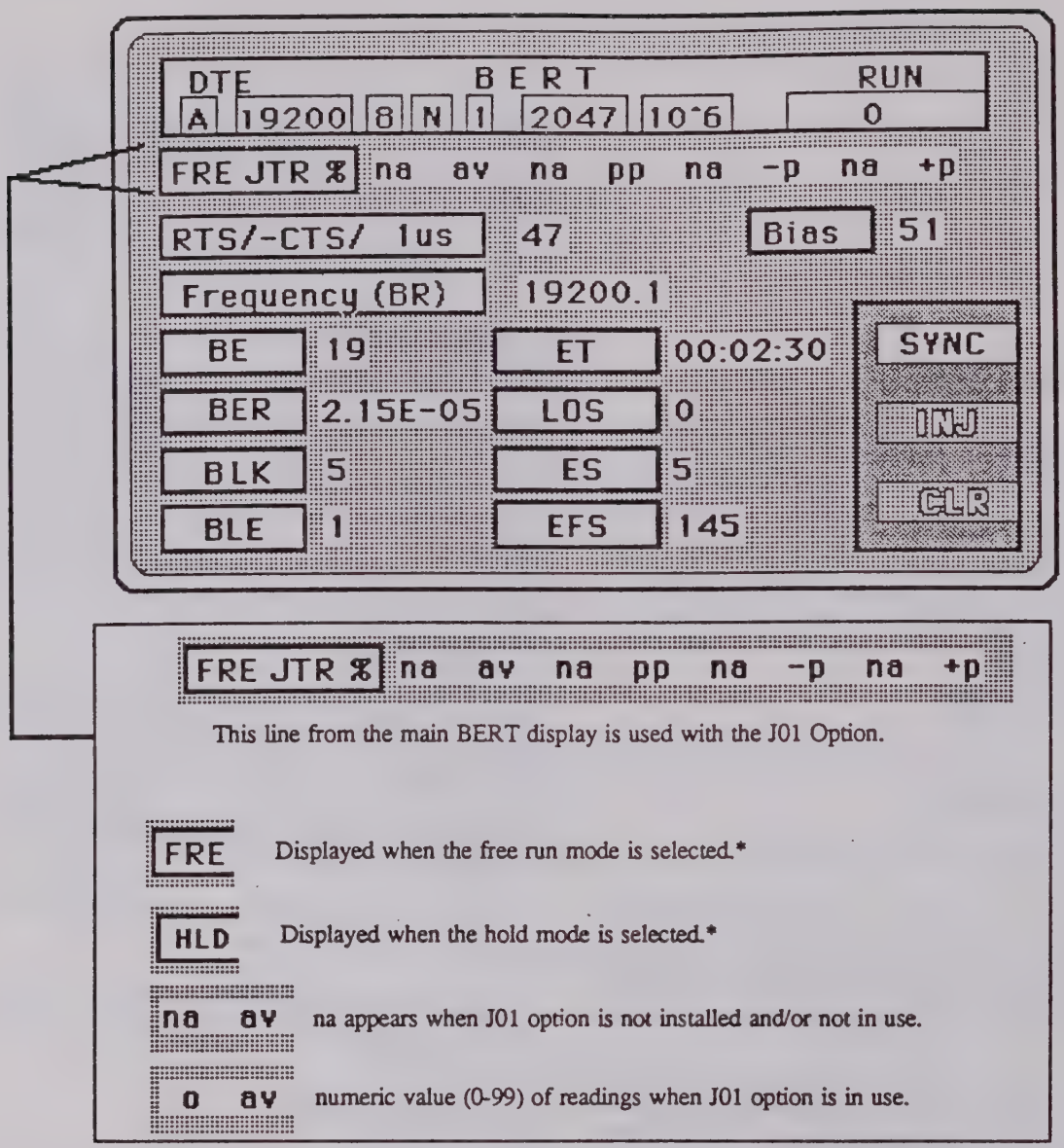
av Represents the average difference between data edges, sampled over the same 1024 or 256 bit period as the **pp**, **+p**, and **-p** readings.

4.0 MAINTENANCE

Since the 5500-J01 option uses an all digital approach, no setup or adjustment is required. An occassional frequency check may be desirable, to insure the calibration of the 18.432 MHz oscillator.

Table 2-1. Model 5500-J01 Specifications

CHARACTERISTIC	SPECIFICATION
FREQUENCY RANGE	75 bps to 72000 bps at standard bit rates.
ACCURACY	± 1.0 %
OFFSET	± 1.0% maximum except for 134.5 and 56000 Hz ± 2.0% at 134.5 and 56000 Hz



* only operator selections available in jitter measurement.

NOTE: For information on all aspects of this display, refer to figure 3-4 in the Operation section of this instruction book.

Figure 3-1. Model 5500-J01 BERT Format

Model 5500-J02

T-Carrier Timing (Clock) Jitter Injection/Measurement Option

1.0 INTRODUCTION

The Model 5500-J02 Jitter Injection/Measurement Option is a factory installed option which provides the 5500 user with jitter measurement and jitter injection capability. This capability is used with T-1 1.544 Mbps Bipolar transmission facilities and equipment. The 5500-J02 option consists of a piggy back circuit card which is plugged into the top of the 5500-624 Framed/Unframed T-1 Interface Module (described in the Option section of this instruction book). This option may be installed in equipment of the following configurations:

Model 5500 main frame -- Revision 4.00 or above.

Software -- Revision 4.11 or above.

Model 5500-624 I/O module -- Revision 1.20 or above.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-J02 Jitter option.

Table 2-1. Model 5500-J02 Specifications

CHARACTERISTIC	SPECIFICATION	
JITTER MEASUREMENT		
Bandlimiting Filter	2 pole high pass/8 pole low pass (10Hz to 40kHz)	
Wideband Jitter Amplitude ("TOTAL JITTER")		
Amplitude range	0.00 to 12.75 ui (unit intervals)	
Amplitude accuracy	± 5% ± 0.05 ui	
Narrowband Jitter Amplitude ("CURSOR AMP")		
Amplitude range	0. 00 to 12.75 ui	
Amplitude accuracy	± 5% ± 0.025 ui	
Narrowband Jitter Filter ("CURSOR FREQ")		
	10Hz to 15kHz	15kHz to 40kHz
Center frequency	± 50 ppm	± 50 ppm
Bandwidth (3 dB)	± 11%	± 11%

Table 2-1. Model 5500-J02 Specifications (Cont.)

CHARACTERISTIC	SPECIFICATION
JITTER GENERATOR	
Amplitude Range	0.00 to 12.75 ui
Amplitude Resolution	
"FAST" Scroll	0.5 ui increment/decrement
"SLOW" Scroll	0.05 ui increment/decrement
Amplitude Accuracy	± 5% ± .05 ui
Frequency Range	10Hz to 40kHz
Frequency Accuracy	± 50 ppm
Frequency Resolution	
"FAST" Scroll (Expand enabled)	106 LOG spaced increments
"SLOW" Scroll (Expand enabled)	>1600 LOG spaced increments

2.1 OPTION HIGHLIGHTS

The JO2 option permits the user to perform the following jitter tests of T-1 equipment and/or facilities:

Measure Jitter

- ¤ Total wideband (10Hz to 40kHz) Jitter Amplitude (to 13 Unit Intervals)
  - ° Peak to Peak unit intervals, or
  - ° Negative peak unit intervals, or
  - ° Positive peak unit intervals.
- ¤ Jitter Spectrum Analysis
  - ° Automatic sweep, 10Hz to 40kHz in 106 LOG steps.
  - ° Numerical readout and easily interpreted graphic display for each of 106 spectral measureaments.
  - ° AT&T jitter specification limit mask displayed with numeric readout.
  - ° Automatic identification of out-of-specification measurements.
  - ° Optional manual control of narrowband spectral measurements.
- ¤ Jitter Measurement Flexibility
  - ° Framed T1
  - ° Unframed T1
  - ° Live traffic, bridged or terminated
  - ° Remote Control

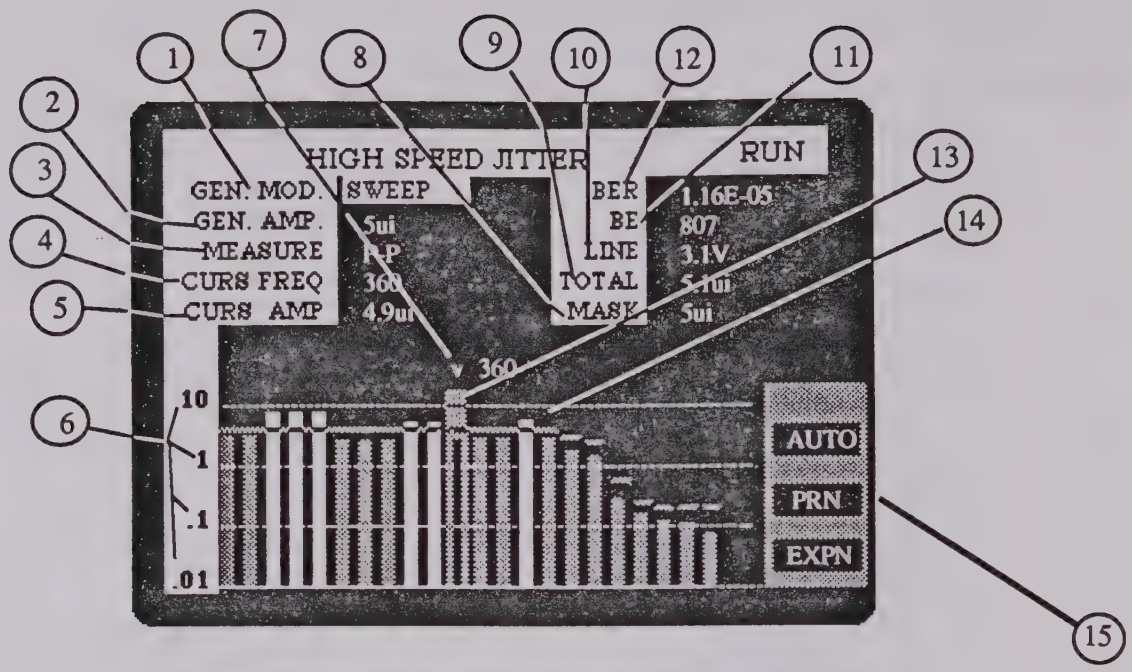
Inject Jitter

- ¤ Sweep AT&T Specification Limit Mask
  - ° Automatic sine sweep, 10Hz to 40kHz, in 106 LOG steps.
  - ° Numeric readout of injected amplitude unit intervals and frequency.
  - ° Simultaneous measurement of received jitter, bit errors, etc.
  - ° Choice of any Model 5500 BERT patterns (QRW is AT&T standard).
  - ° Optional manual control of all jitter injection parameters.
    - * Sine wave or triangle modulation
    - * 1600 step frequency resolution (fast/slow cursor frequency control)
    - * .05 unit interval amplitude resolution (fast/slow scroll)
    - * 12.75 unit intervals maximum
- ¤ Jitter Injection Flexibility
  - ° Framed T1 (D4)
  - ° Unframed T1
  - ° AMI or B8ZS
  - ° Analog modulation input
  - ° Remote control

3.0 OPERATION

3.1 CONTROLS AND INDICATORS

Figure 3-1 presents the 5500 Display and Controls with the JO2 option installed. Table 3-1, which is keyed to figure 3-1, provides a detailed description of the functions of the various display items and softkey controls.



15 SoftKeys are redefined as a function of selected GEN. MOD. operating modes

GEN. MOD.
SWEEP

GEN. MOD.
SIN
TRI
OPT
OFF

AUTO	Enables auto sweep of jitter tolerance mask.	FAST	Enables coarse CURS FREQ resolution and coarse GEN. AMP. resolution.
PRN	Activate to print out a bar graph of the entire measured jitter display graph	PRN	Activate to print out a bar graph of the entire measured jitter display graph.
EXPN	Compressed display mode.	EXPN	Compressed display mode.
MAN	Enables manual control of CURS FREQ with interlocked auto AMP control.	SLOW	Enables fine CURS FREQ resolution and fine GEN. AMP. resolution.
	Indicates Printer Port not enabled.		Indicates Printer Port not enabled.
EXPN	Enables high resolution display mode (1/5 of total spectrum displayed).	EXPN	Enables high resolution display mode (1/5 of total spectrum displayed).

Figure 3-1. 5500 Display and Controls

Table 3-1 Model 5500-JO2 Controls and Indicators

INDEX NUMBER	DISPLAY	FUNCTION
1	GEN. MOD.	GENERATOR MODULATION, selects the type of Jitter modulation to be injected in the transmit jitter clock (note: Jitter modulation of the transmit data requires selection of CLOCK SOURCE = JIT CLK on the BERT FORMAT MENU). SWEEP, SIN, TRI, OPT and OFF are the selection options.
1a	GEN. MOD.	**SWEEP** - automatically sweeps the AT&T jitter tolerance mask per figure 14 of Bell System Technical Reference PUB62411. The frequency of the JIT CLK sinusoidal modulation is automatically swept from 10 HZ to 40 kHZ, while automatically controlling the amplitude of the JIT CLK modulation to that specified by the AT&T jitter tolerance mask: 10 HZ to 500 HZ = 5 ui (unit intervals) 500 HZ to 8 KHZ = -8.5 dB/Octave to 0.1 ui @ 8 KHZ 8 KHZ to 40 KHZ = 0.1 ui The SWEEP may be halted at any point by activating the AUTO softkey to MAN. When in the SWEEP MAN mode, the CURS FREQ may be manually adjusted via the SELECT key (the GEN. AMP. will automatically track the AT&T mask). When the AUTO/MAN soft key is cycled from AUTO to MAN and back to AUTO, the direction of the sweep will be reversed. Resolution of the GEN. AMP. control is .05 ui, and the GEN. AMP. will automatically be set to the .05 ui increment closest to the actual MASK limit at the CURS FREQ (CURSOR FREQUENCY). The actual MASK limit is displayed (5th parameter down on right side) to two significant decimal places.
1b	GEN. MOD.	**SIN** - Selects Sinewave Jitter Modulation. The amplitude of the sinewave modulation is controlled by scrolling the GEN. AMP. with the SELECT Key. In this mode, the amplitude of the jitter moduation is not forced to the AT&T spec limit, and the jitter moduation may be adjusted from 0 ui to 12.75 ui in .05 ui steps (FAST/SLOW soft key = SLOW). Note that the functions of the three soft keys (at the lower right side of the CRT) are redefined when the GEN. MOD. mode is changed from SWEEP to one of the four alternate modes (see figure 3).
1c	GEN. MOD.	**TRI** - Selects Triangle wave Jitter Modulation. The peak-to-peak amplitude of the triangle wave jitter modulation is controlled the same as for sinewave modulation. The modulation wave form is a 50% duty cycle linear triangle function having odd harmonic content decreasing at 12 dB per octave.
1d	GEN. MOD.	**OPT** - Selects an OPTIONAL Jitter Modulation Waveform. The jitter waveforms are specified by a PROM memory device with 100 points per period below 15 KHZ, and 16 points per period above 15 KHZ. One section of the PROM is allocated for an optional modulation waveform. (A unique waveform may be specified by the user. A one time charge is required. Consult Phoenix customer service for delivery and price.) The OPT waveform in unmodified production hardware is a 50% duty cycle square wave.

Table 3-1 Model 5500-JO2 Controls and Indicators (Cont.)

INDEX NUMBER	DISPLAY	FUNCTION
2	GEN. AMP.	GENERATOR AMPLITUDE, displays the amplitude of the jitter modulation in unit intervals (ui) peak to peak. This is the magnitude of jitter being injected in the transmitter data at the model 5500 T1 TX output jack. In the GEN. MOD. SWEEP mode, this amplitude is automatically set to the level defined by the AT&T jitter tolerance MASK limit (to the closest .05 ui increment) at the selected CURS FREQ. In the GEN. MOD. SIN, TRI or OPT modes, this amplitude is adjustable via the SELECT key from 0 ui to 12.75 ui in .05 ui steps (FAST/SLOW soft key = SLOW) or in 0.5 ui steps (FAST/SLOW soft key = FAST).
3	MEASURE	Displays the selected jitter measurement mode: P - P Peak to Peak jitter amplitude +P average to positive peak jitter amplitude -P average to negative peak jitter amplitude (CURS AMP (#5) and TOTAL (#9) are P-P, +P, -P as indicated above.)
4	CURS FREQ	CURSOR FREQUENCY, displays the frequency of the generator jitter modulation in the GEN. MOD. SWEEP SIN TRI or OPT modes; and displays the selected measurement frequency when the GEN. MOD. is OFF . The CURS FREQ is indicated on the GRAPH display by the tall (off scale high), wide bar (see item 13 on figure 3). The CURS FREQ is adjustable via the SELECT key over the range of 10 HZ to 40 KHZ. The frequency increments and graph scale are approximately logrithmic. Frequency selection resolution varies depending upon the combination of FAST/SLOW and EXPN (EXPAND) mode selections. All automatic SWEEP measurements are made with approximately 10% frequency increments (i.e. 10, 11, 12, 13 ... 20, 22, 24, ... etc.). When the EXPN function is disabled, the graph data is condensed to fit all data from 10 KZ to 40 KHZ onto the CRT screen. The data continues to be obtained at the frequency resolution of the "EXPANDED" mode; however the data is compressed by displaying the highest measured jitter amplitude for 5 contiguous frequency increments as one bar at a single frequency. That is, the EXPN disabled mode results in a 5 to 1 compression of the graph data. This compression is only for the purpose of condensing the data for 106 discrete measurements to be displayed as 22 data points on one screen. All measurement sweeps are performed at 106 discrete frequency increments, all of which may be displayed by scrolling the CURS FREQ in the EXPN mode. No data is lost by switching between the compressed screen and the expanded screen modes - all graph data is retained in memory in the high resolution mode (106 discrete frequency data points). The FAST/SLOW soft key in the SLOW mode results in a frequency resolution of 1/16th that of the FAST mode (i.e. 10, 10.0625, 10.125, ..., 20, 20.125, 20.25, ... etc.), for a resolution step increment of less than 1% in the EXPN SLOW mode of CURS FREQ selection.
5	CURS AMP	CURSOR AMPLITUDE, displays the amplitude of the measured jitter of the received data at the CURS FREQ. This is a narrow band measurement (1/3 octave filter bandwidth) and is given in unit intervals, (ui).

Table 3-1 Model 5500-J02 Controls and Indicators (Cont.)

INDEX NUMBER	DISPLAY	FUNCTION
6	GRAPH VERTICAL SCALE	The vertical scale for the graph display is logrithmic with greater than three decades dynamic range (>60dB). The display range is from .01 unit intervals to 12.75 unit intervals with horizontal dashed lines identifying the .01, .1, 1 and 10 unit interval amplitudes.
7	v360	The "v" character identifies the graph bar corresponding to the narrow band measurement currently being processed. The measurement frequency is displayed just to the right as in "v 360". In the jitter measurement only mode, when jitter injection is disabled (GEN. MOD. = OFF), continuous readout of a single frequency spectral amplitude is provided via the CURS FREQ and CURS AMP displays, and simultaneously the spectrum analyzer sweeps the displayed frequency band and continuously updates the amplitudes of the measured spectral components. The "v" character (followed by numeric display of frequency) all move from left to right indicating the measurement in progress. With the EXPN function disabled, all 106 measurements will be updated, but the display will be compressed by a factor of 5 to 1. The high resolution results of the complete spectral sweeps may be displayed at any time by activating the EXPN to enable and using the CURS FREQ control to move to the desired area of the spectrum. However, once in the EXPN enabled mode the continuous sweep update of the spectrum is limited to that portion of the spectrum currently displayed (as is clearly indicated by the "v" character and trailing frequency readout).
8	MASK	The amplitude of the AT&T jitter tolerance MASK limit at the CURS FREQ is displayed in unit intervals (ui). This readout is automatically updated to track the selected cursor frequency. This data point is provided as reference data for assessing performance margins at individual frequencies across the spectrum from 10 HZ to 40 KHZ.
9	TOTAL	The amplitude of the wideband jitter amplitude, including all frequency components between 10 HZ and 40 KHZ, is continuously measured and displayed as TOTAL unit intervals of jitter. This measurements is P-P (peak to peak), +P (positive peak), or -P (negative peak) as selected and indicated by the item 3. MEASURE mode.
10	LINE	The approximate amplitude of the bipolar waveform at the RX jacks of the model 5500 T1 module is displayed in volts, average to peak. This measurement is obtained by digitizing the AGC (Automatic Gain Control) voltage level of the Automatic Line Build Out (ALBO) in the line receiver circuit. A software calibration curve converts this measurement to the corresponding line voltage amplitude.
11	BE	BIT ERRORS, displays the number of bit errors measured by the Model 5500 Analyzer. This is one of two programmable parameter display blocks on the high speed jitter menu screen. Any of the greater than 2 dozen available parameter blocks may be selected for display in this position.

Table 3-1 Model 5500-J02 Controls and Indicators (Cont.)

INDEX NUMBER	DISPLAY	FUNCTION
12	BER	BIT ERROR RATE, displays the measured bit error rate. This is one of two programmable parameter display blocks. The CURSOR positioning and SELECT keys are used to scroll through all available display parameters in each position.
13		The tall, wide bright bar is the cursor bar which highlights the measurement in progress at the selected CURS FREQ. Note that the amplitude of the cursor frequency measurement is indicated by a dark inverse video bar within the bright cursor bar.
14		This stair-stepped line is the Graph of the AT&T Jitter Tolerance limit MASK.
15	SOFT KEYS	As indicated in the chart below the display screen of figure 3, the soft key functions are re-defined for different measurement modes. ° The AUTO/MAN soft key controls the frequency sweeps of the jitter generator in the GEN. MOD. SWEEP mode. This soft key becomes the FAST/SLOW control for both frequency and amplitude in all other modes. ° The PRN function will not be available on this menu if the printer port is not enabled on the Remote Port Set Up Menu. ° See items 1 and 7 for explanation of the interactions of AUTO/MAN and EXPN soft keys.

3.2 THEORY OF OPERATION

The JO2 Option consists of two independent hardware subsections: (A) Jitter Measurement circuitry and (B) Jitter Injection circuitry. The jitter measurement and jitter injection functions may be used interactively or independently as the situation requires.

3.2.1 Theory of Operation - Jitter Measurement

A block diagram of the Jitter Measurement circuitry is shown in figure 3-2. The phase of the received clock (RCV CLK) from the T1 Interface Board is measured against the phase of the long term average of the received clock (AVG RCV CLK) by an analog phase comparator. Both clocks are divided by 16, before phase comparison, to allow detection of phase jitter of greater than 10 unit intervals peak to peak. The RCV CLK LONG TERM AVERAGER consists of a crystal controlled VCO/Phase Lock Loop with a low pass loop filter that allows the VCO to lock to the long term average of the RCV CLK without transferring the RCV CLK phase jitter components (above 10 HZ) to the AVG RCV CLK reference signal for the phase comparator. The analog output of the phase comparator represents the demodulated phase jitter of the RCV CLK (above 10 HZ). This phase comparator output is band limited by a two pole high pass/8 pole low pass filter for the frequency band of interest: 10 HZ to 40 KHZ. This band limited analog demod phase jitter signal is accessible at the phase jitter receive monitor BNC connector (PHASE JITTER RX MON) on the rear of the Model 5500-624 interface module.

Two tuneable solid state 1/3 octave filters are used to perform the spectrum analysis of the receive clock phase jitter demodulation signal: (A) a transversal filter covers the band from 15 KHZ to 40 KHZ, and (B) a switched capacitor filter covers the band from 10 HZ to 15 KHZ. The 2 pole high pass/8 pole low pass filter provides anti aliasing band limiting for the transversal filter; and a separate low band ANTI ALIAS FILTER network (actually a 2 pole low pass active filter with 4 selectable break points) performs anti aliasing for the low band switched capacitor filter. A frequency synthesizer sets the tuned cented frequency of the digital filters by controlling the filter clock drive frequency. The outputs of these two filters are selected through a variable gain network for peak detection. The amplitude of positive peak, negative peak, or peak to peak phase jitter for both the "total" (10 HZ to 40 KHZ band width) and the selected narrow band frequency is then digitized by an analog to digital converter (ADC) and made available to the data bus. Auto ranging of the gain selection, ADC sampling intervals, filter and peak detector dwell times, narrow band filter tuning and other special timing and control signals relating to the dynamics of the spectrum analyzer function are implemented by software control loops via the bi-directional data bus interface. The automatic line build out (ALBO) level from the T1 line receiver circuit is also digitized by the ADC to provide an indication of the received bipolar signal amplitude. This d.c. level is proportional to the gain required to equalize (gain and phase compensate) the received waveform, and a software calibration curve converts the ALBO voltage measurement to the corresponding peak amplitude of the bipolar waveform (3.0 volts peak is nominal).

3.2.2 Theory of Operation - Jitter Injection

A block diagram of the Jitter Injection circuitry is shown in figure 3-3. The Model 5500 analyzer provides a 1.544 MHZ crystal oscillator clock which the JO2 jitter option board uses as a reference clock for the phase jitter modulator. This reference clock is divided by 20, and the output of the jitter modulator VCO is also divided by 20 to allow phase modulation magnitudes in excess of 13 unit intervals. The two divided-by-20 clocks are input to a digital phase comparator which generates a pulse width modulated error signal. The error signal is low pass filtered and applied to one of the VCO control voltage inputs to establish VCO frequency and phase lock to the reference 1.544 MHZ clock. A digital waveform synthesizer, consisting of a Frequency Synthesizer, a Waveform PROM (Programmable Read Only Memory), a Modulation DAC (Digital to Analog Converter), a Gain DAC, and an Accentuation filter generates a modulation waveform for application to the VCO voltage control network. The Waveform PROM defines the modulation waveform amplitude for one complete cycle (or period) with a resolution of 100 points per cycle below 15 KHZ, and 16 points per cycle at 15 KHZ and higher.

The JO2 Waveform PROM defines a Sinewave and a Triangle Wave (50% duty cycle, linear); and includes provisions for a third OPTIONAL waveform. The standard production hardware is delivered with a 50% duty cycle square wave in the "OPT" section of the PROM. (Custom programming of the third "OPT" waveform is available for a one time charge.)

Amplitude and frequency of the injected phase jitter modulation is software controlled via the data bus. The resulting JITTERED CLK is menu selectable for use as the transmit clock source for the Bit Error Rate test patterns generated by the Model 5500. The phase jittered logic data sequences are than encoded into AMI or B8ZS, framed or unframed bipolar signals for transmission on standard T1 digital communication networks.

An external analog phase jitter modulation input connector is accessible at the rear of the Model 5500-624 I/O module. The BNC connector is labeled PHASE JITTER TX INJ. Connection of a general purpose

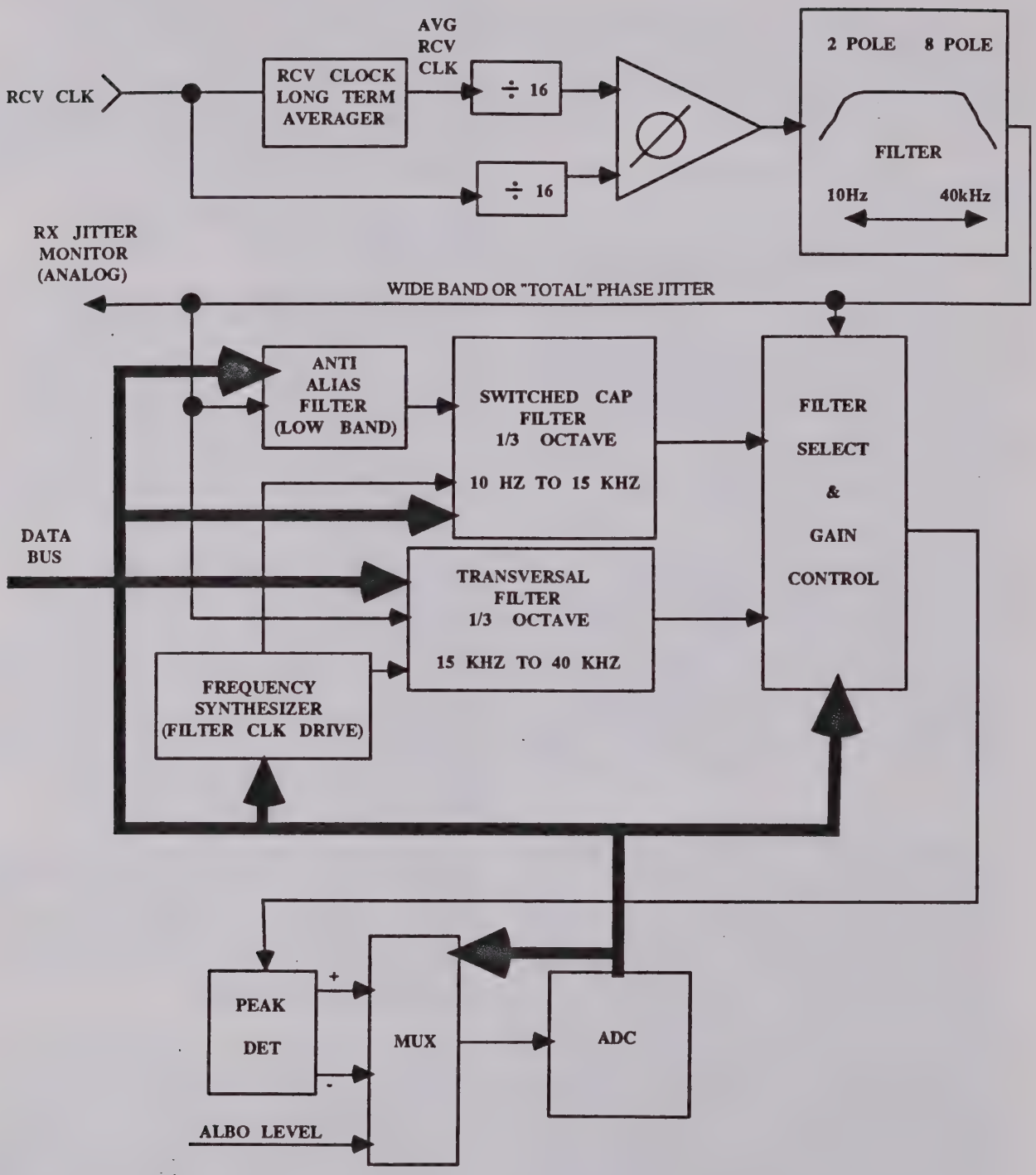


Figure 3-2. Jitter Measurement Block Diagram

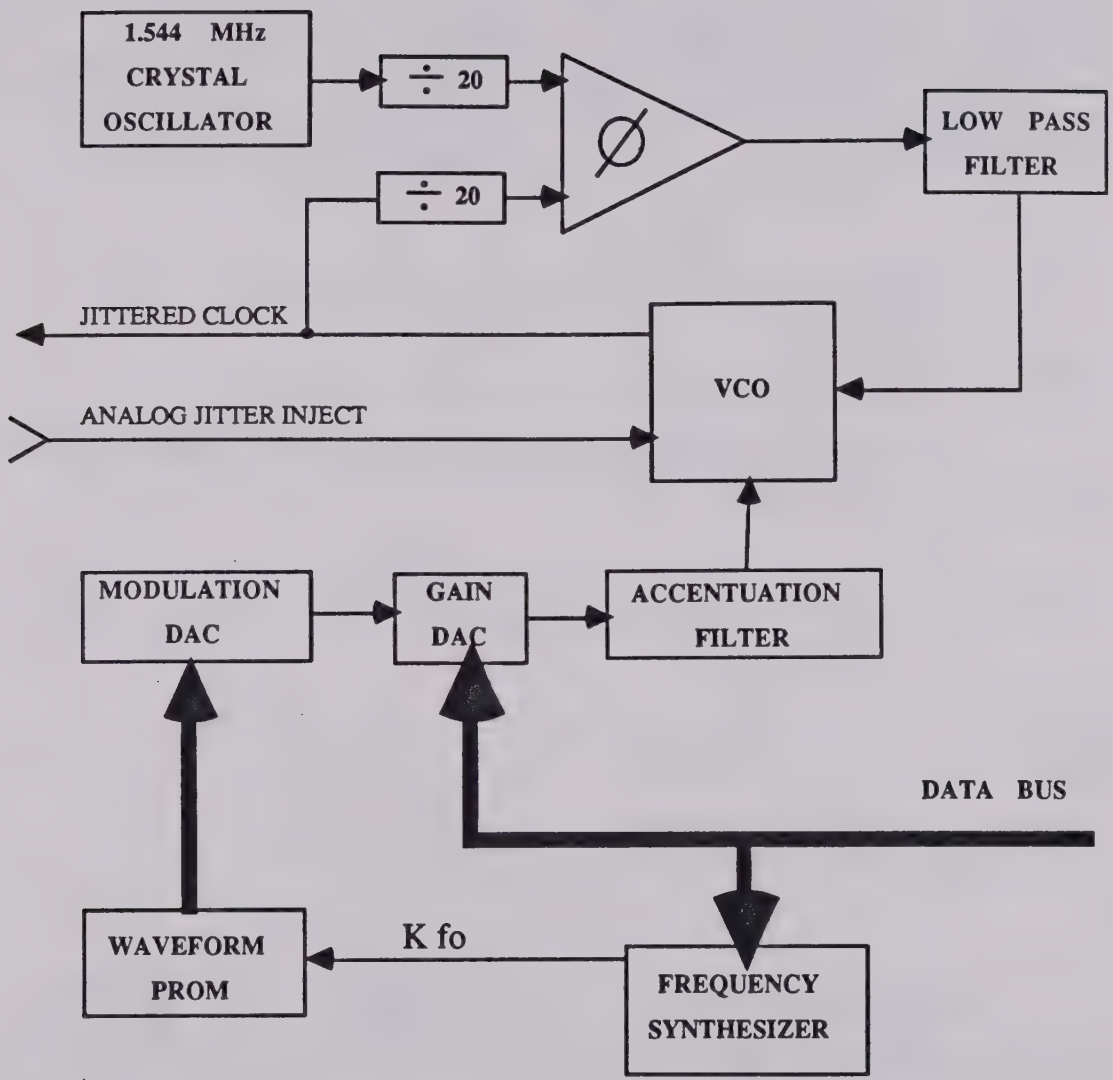


Figure 3-3. Jitter Injection Block Diagram

waveform generator allows external control of phase jitter modulation amplitude and frequency. The JO2 phase jitter measurement features should be used (with the 5500 in "LOOP" mode) to calibrate the external modulation signal. This is accomplished by simply adjusting the amplitude and frequency of the external modulation signal to achieve the desired phase jitter. The external modulation will be superimposed with the selected internal modulation. The use of complex waveforms, random noise, etc. is perfectly acceptable. In fact, the Phoenix JO2 option has been used to successfully phase modulate and demodulate voice communications over the 1.544 MHZ data circuit.

3.3 ILLUSTRATIONS OF T1 PHASE JITTER

Figures 3-4 and 3-5 illustrate two examples of phase jitter as it would appear on the T1 bipolar waveforms as observed via an oscilloscope synchronized to the originating, stable, non-jittered timing source (1.544 MHZ). Two primary causes of phase jitter are (1) frequency offset of span line repeater clock recovery tuned circuits, and (2) phase modulation in the clock recovery/regeneration circuits of multiplexers and de-multiplexers which necessarily must deal with phase jitter associated with the use of stuff bits and/or elastic stores employed to achieve network synchronization.

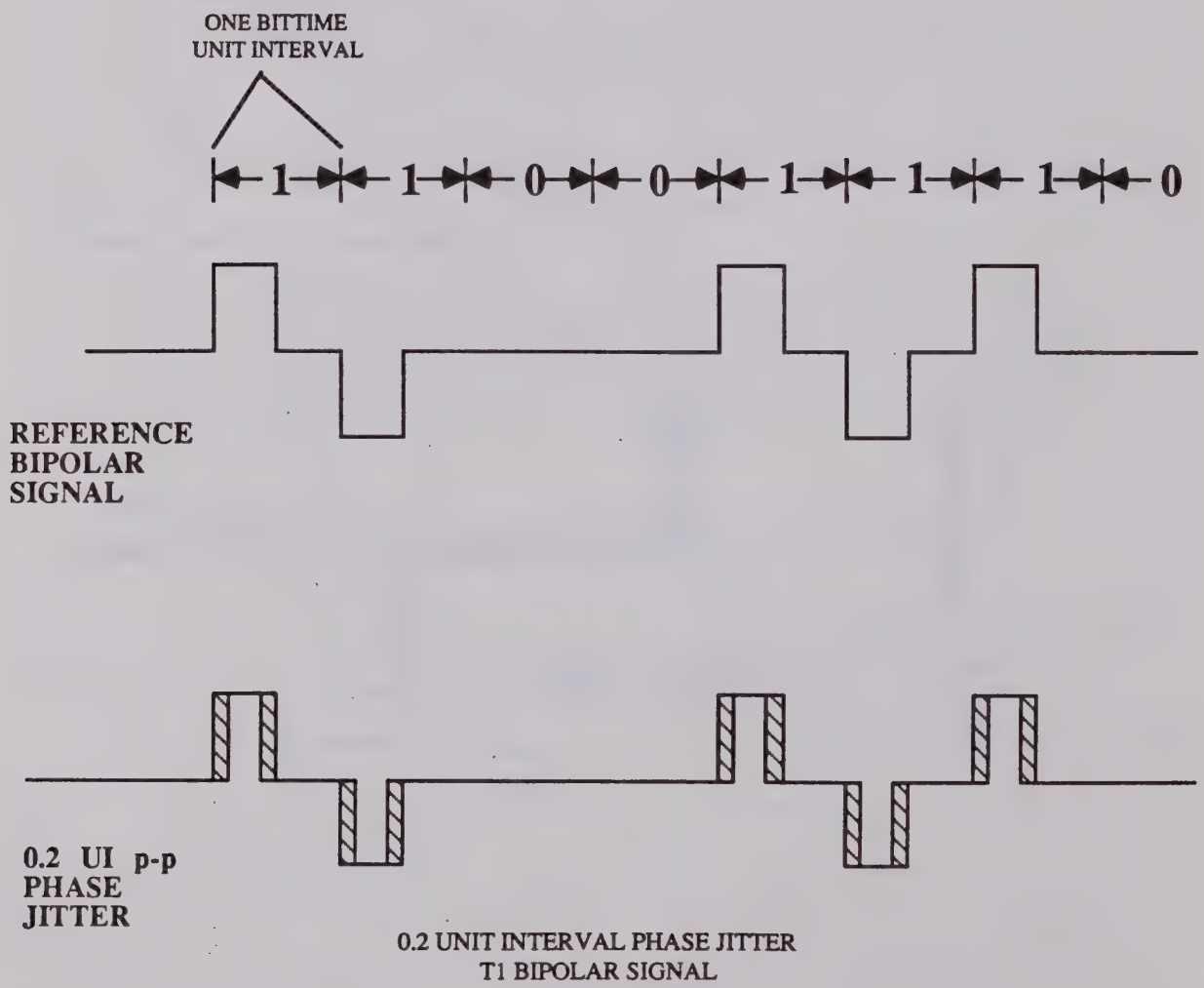
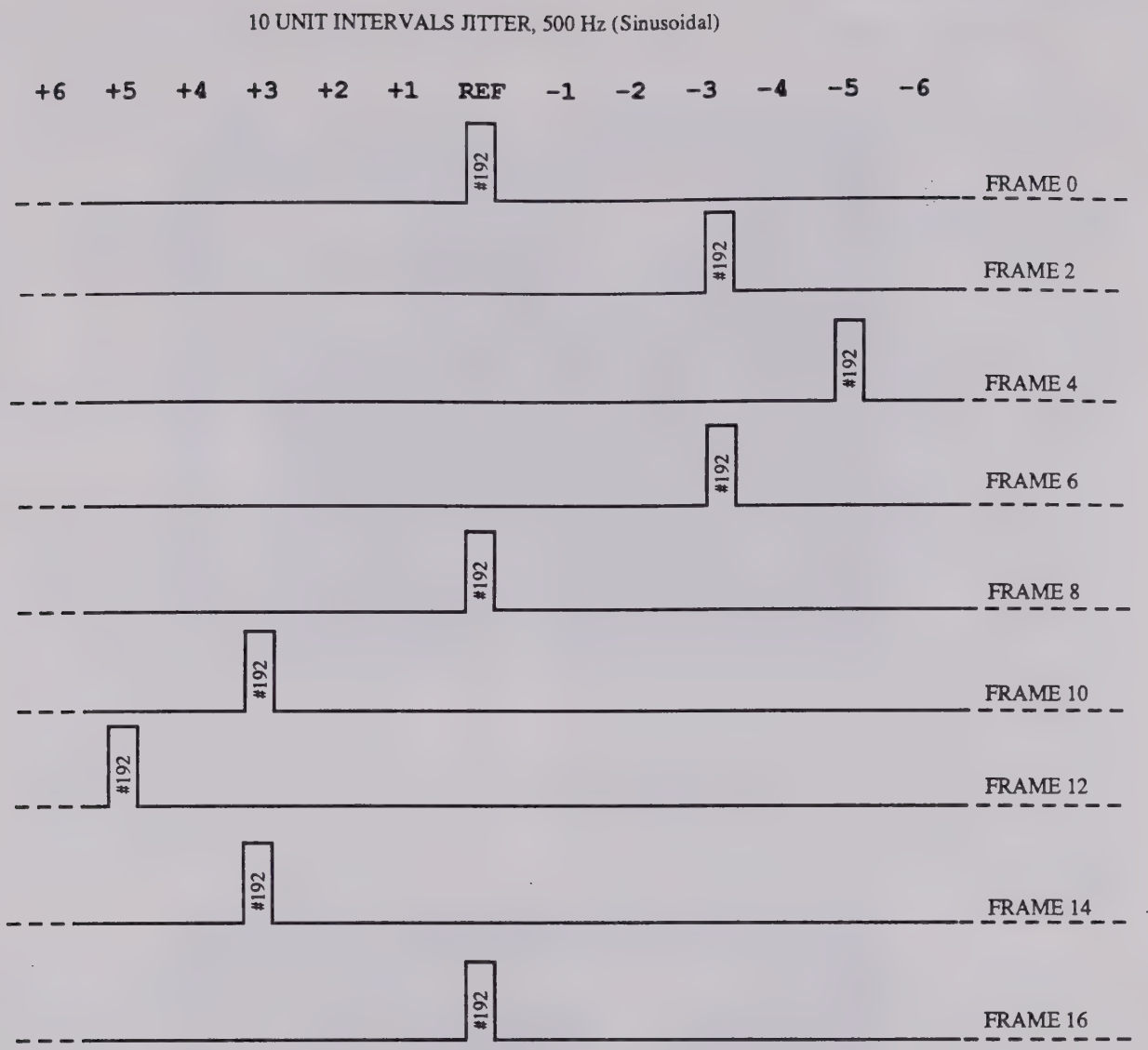


Figure 3-4. Phase Jitter on T! Bipolar Signal



$$\frac{\text{FRAME RATE}}{\text{JITTER FREQUENCY}} = \frac{\text{8000 FRAMES/SEC}}{\text{500 CYCLYES /SEC}} = \text{16 FRAMES/JITTER CYCLE}$$

@ 500 HZ JITTER FREQUENCY

Isolated T1 bipolar pulse No. 192
T1 Frame rate 8000 Hz
193 bits/frame

Figure 3-5. Isolated Pulse Jitter Representation

4.0 JO2 APPLICATION

The following paragraphs provide test set up procedures and examples for using the Model 5500-JO2 high speed jitter option.

4.1 Measure Jitter, Live Traffic, Framed or Unframed

Phase Jitter of a T1 bipolar digital data line may be measured with the JO 2 option, regardless of the transmitted data pattern (LIVE Traffic, BERT PATTERN, KEEP ALIVE SIGNAL, YELLOW ALARM,... D4 FRAMED or NOT D4 FRAMED). When the T1 bipolar signal is connected to the RX Input jack on the rear of the Model 624 interface module, the JO2 option card will recover clock, establish a long term frequency and phase average reference clock, and measure the amplitude and frequency spectra of the received clock phase jitter. This measurement may be accomplished in either the BRDG (Bridged) mode or the TERM (Terminated) mode. For "LIVE" traffic, the Model 5500 analyzer will not achieve SYNC (pattern synchronization) because a known pseudo random test pattern will not be present. Likewise, BE (Bit Error) , BLKE (Block Errors), etc. will not be detected. However, if trouble is reported or suspected on an in service T1 line, the line may be tested for FRAME errors, B2 alarm status, S Bit errors, BPV's (Bipolar Violations), line level and phase jitter without interrupting or interferring with the live T1 traffic. The following set-up procedure will accomplish testing of T1 live traffic:

A) On the Framed T1 FORMAT Menu:

1. Select FRAME [ENABLE]
2. Activate [BRDG] or [TERM] softkey as desired.
3. De-Activate [LOOP]

B) On the HIGH SPEED JITTER menu:

1. Select [GEN.MOD.] = Off
2. Select [GEN.AMP.] = O ui
3. Select [MEASURE] = P-P
4. On the upper right side of this menu there are 2 programmable parameter blocks. Using the CURSOR control keys and the SELECT key, select any 2 test parameters for display, for example:

RBPV	Ø	Received Bipolar Violations
ALRM	. . . . . S . F	The "F" would indicate FRAME errors, the "S" would indicate S - Bit errors.
ALRM	. . . . .	If all Framing bits are correct, the ALRM parameter will be a row of dots.

5. Observe the [TOTAL] jitter amplitude. This is a measure of the total wideband (10HZ to 40KHZ) peak-to-peak jitter amplitude in unit intervals (ui).

6. To determine whether the measured TOTAL jitter is above or below allowable limits, observe the graph display of jitter amplitude for each of 106 narrow band measurements. Any spectral components above the AT&T MASK limit will be highlighted as a bright magnitude bar. Using the CURS FREQ (CURSOR FREQUENCY) control move the graph cursor (tall, wide bar) to coincide with any detected spectral component and observe the numeric amplitude readout beside CURS AMP (CURSOR AMPLITUDE). Compare this number to the MASK value which identifies the numeric limit at the CURS FREQ.

7. An example of a phase jitter measurement is illustrated in figures 4-1 and 4-2. In Figure 4-1, the EXPAND function is disabled and the entire spectrum from 10HZ to 40 KHZ is displayed. In this mode each bar actually represents the results of 5 discrete spectral tests - with the highest jitter measurement in the band of 5 frequencies determining the height of the bar for that group of measurements. This compressed display mode quickly identifies the approximate frequency of any out-of-limits spectral components anywhere in the specified band width. By enabling the [EXPN] function, and adjusting the graph cursor position (by scrolling the CURS FREQ), the high resolution graph mode (as illustrated in fig 4-2) reveals that the measured jitter (for this example) is concentrated at two frequencies. The two frequencies and the amplitudes at each frequency are determined by moving the cursor to each peak and observing the CURS FREQ and CURS AMP numeric readouts.

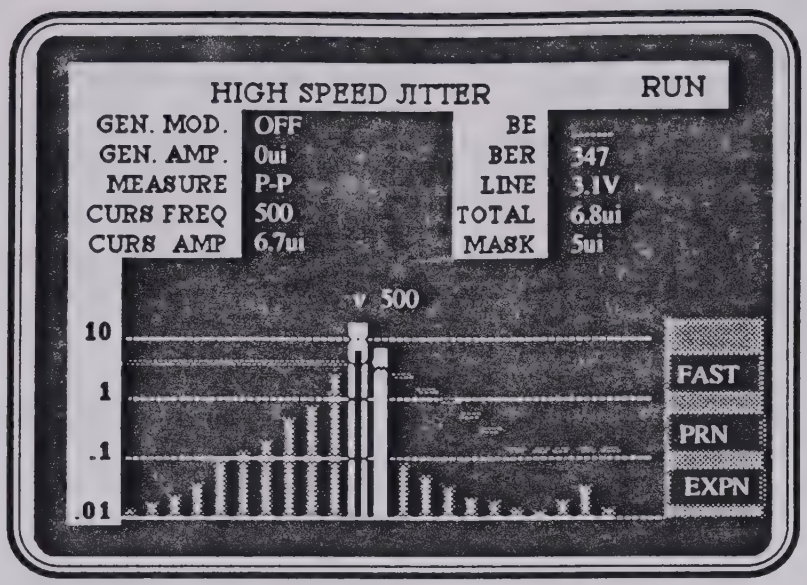


Figure 4-1. Phase Jitter Measurement
Expand Function Disabled

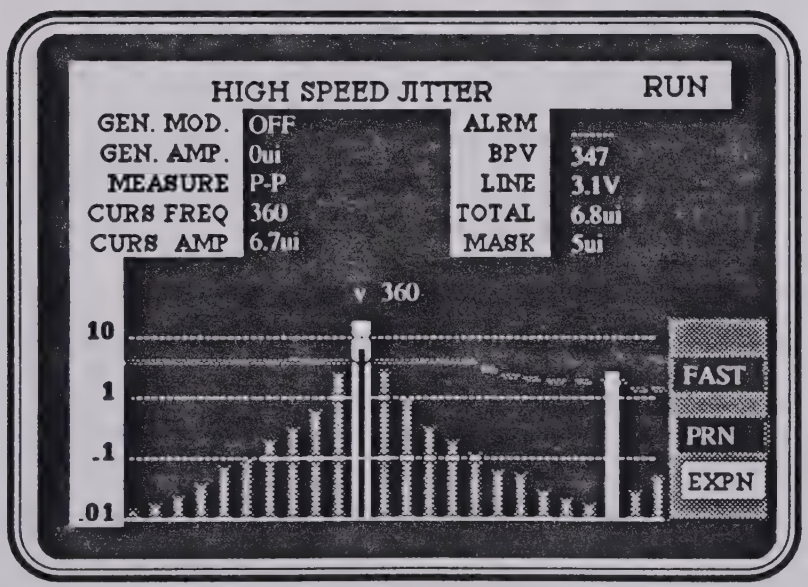


Figure 4-2. Phase Jitter Measurement
Expand Function Enabled

In addition, notice that the "v" character (followed by a number) continues to scroll across the screen above the bar graph as the graph data is continuously updated with new measurements. The number after the "v" indicates the frequency at which the current measurement update is being performed (i.e. "v 330" would indicate a measurement at 330HZ and the bar graph directly below the "v" represents the amplitude of the spectral component at that frequency. In the EXPAND mode, only that portion of the spectrum on the screen (approximately 1/5th of the 10HZ to 40 KHZ spectrum) is continuously updated, as indicated by the movement of the "v" character. When the EXPAND mode is disabled, the entire spectrum is updated - but remember that each bar represents the results of 5 individual spectral measurements. 106 spectral measure-ments are made in one complete sweep and these are compressed into 22 lines with EXPN disabled. The data is "uncompressed" for high resolution display when EXPN is enabled.

4.1.1 Interpreting the Data

The degree of randomness and the one's density of the digital data sequences transmitted over the measured T1 line will have an effect on the amplitude of the measured spectra due to (A) the tuning errors and dynamic response characteristics of the clock recovery circuits in repeaters, multiplexers, CSU's etc, and (B) the intersymbol modulation associated with the phase distortion which occurs in the T1 cables and in the span line repeaters and Model 5500 receiver ALBO's (Automatic Line Build Outs). The AT&T jitter tolerance spec limits are based on test measurements using the standard Bell System Quasi-Random Test Signal (or Quasi Random Word -"QRW"). This signal has 50% ones density and no strings of zeroes greater than 15 (D4 framed; 14 zeroes max when un-framed). The Model 5500 permits the correlation of phase jitter data with BPV and Frame error data on live traffic and also facilitates the characterization of jitter tolerance and jitter transfer function performance in accordance with the AT&T specifications. Futhermore, the use of USER specified test patterns facilitates testing with worst case one's density (12.5%) and evaluation of clock recovery circuit dynamics and design margins by subjecting the receivers to excessively long strings of zeros with varying degrees of one's density.

4.2 Inject Jitter, Evaluate Jitter Tolerance

When measuring jitter tolerance of a T1 facility or span line or its component parts such as repeaters, multiplexers, CSU's and Bit Error Rate Testers! (the test sets need to be better than the facilities they are testing!), the object is to stress the system with phase jitter modulation of the data transmitted into the facilities (or component parts) and observe the ability of the facilities to transport the data without incurring unacceptable levels of bit errors, sync losses, framing errors, etc. The Model 5500 Analyzer with Model 624 Framed T1 module and JO2 High Speed Jitter option provides the capability to inject a controlled phase modulation onto a standard T1 bipolar interface signal. The amplitude and frequency of the phase modulation may be controlled to determine the threshold of susceptibility to phase jitter over the phase modulation frequency range of 10HZ to 40 KHZ. The [GEN.MOD] SWEEP mode provides for an automatic sweep of the AT&T jitter tolerance mask (per PUB 62411, figure 14). In this mode, phase jitter modulation at the MASK level is injected at each of 106 frequencies (at one frequency at a time) logarithmically spaced across the spectrum at approximately +10% increments. As the jitter modulation sweep is continuously repeated, the Model 5500 performs a continuous bit error test of the bipolar T1 signal transported through the facility or equipment under test and returned to the RX input jack of the Model 624 interface module. If bit errors, sync losses, BPV's, framing errors, etc. are detected at a given area of the spectrum, then the [GEN.MOD.] mode may be switched to the manual SINEwave mode to determine the level of susceptibility at the specific frequencies of interest. In this mode the [GEN.AMP] level of phase jitter modulation may be raised or lowered to assess the degree of phase jitter susceptibility (i.e. Bit Error Rate versus modulation level; or threshold of induced errors). The [GEN.MOD.] mode also allows the use a TRI angle wave modulation (odd harmonic spectral content decreasing at 12dB/Octave). An external analog TX INJ Phase Jitter modulation input allows the use of random noise generators and/or waveform generators to faciltiate testing with more complex phase jitter modulation waveforms.

The following set-up procedure and display examples will illustrate the jitter tolerance test capabilities of the JO-2 option:

A) On the FRAMED T1 FORMAT menu:

1. Select LINE CODE [AMI] or [B8ZS], as required.
2. Select FRAME [ENABLE] or [DISABLE], as required
3. Select PATTERN [QRW] or other pattern as required.
4. Select BLOCK SIZE [10^6]
5. Select BLOCKS [0]
6. Set BPV INJ RATE and LOGIC ERR RATE as desired

7. Select CLOCK SOURCE [JIT CLK]

Note: If the phase modulated JITTER CLOCK is not selected as CLOCK SOURCE, the transmitted bipolar signal will not be phase jittered.

8. Select AUTO RESYNC [ENABLE]

9. Set SOFTKEY functions to:

[BRDG] (Disabled)

[TERM] (ENABLED) - RX Input Terminated in 100 ohms

[LOOP] (DISABLED)

B) On the HIGH SPEED JITTER menu:

1. Select [GEN MOD] = SWEEP

2. [GEN AMP] is automatically controlled by the Model 5500 analyzer

3. Select [MEASURE] = P-P

4. [CURS FREQ] is automatically swept from 10 HZ to 40 KHZ in 106 log steps

5. [CURS AMP] will display the amplitude of the measured jitter on the RX input signal. This is a measure of the jitter transfer function which may or may not have direct correlation with the jitter tolerance of the facilities under test. For example, the "Q" of the clock recovery LC tank circuit in a typical repeater will affect the jitter tolerance of the repeater and the jitter attenuation characteristics of the repeater. If the "Q" is relatively "low", the jitter tolerance may be relatively "high" because the jittered clock can quickly pull the phase of the LC tank oscillator to track the phase jitter, resulting in little reduction or attenuation of the phase jitter in the regenerated data. Conversely, if the "Q" is relatively "high", the jitter tolerance may be relatively "low" because the jittered clock cannot quickly pull the phase of the high Q LC tank to track the phase jitter. This high "Q" clock recovery circuit would offer relatively high attenuation of high frequency jitter. That is, high "Q" clock recovery might result in poor jitter tolerance but good jitter attenuation for its limited jitter range; and low "Q" clock recovery might result in good jitter tolerance but very little jitter attenuation (also poor margin for excessively long strings of zeros in the data pattern). The best repeater circuits will either make a compromise of the two parameters or (for more $) use more complex circuitry such as rate buffers, long term averaging clock de-jitter circuits, etc., to optimize both parameters (i.e. high jitter tolerance and removal of all high frequency jitter in the regenerated clock). The point is, the jitter transfer function is a very meaningful parameter but does not necessarily have consistent correlation with jitter tolerance. Jitter transfer function testing is illustrated in the next example (see section 4.3).

6. On the upper right side of the HIGH SPEED JITTER menu there are 2 programmable parameter blocks. Using the CURSOR control keys and the SELECT key, select 2 test parameters for display, for example:

[BE]	Ø
[BER]	Ø

7. In the event errors were induced during initial set up of this test, it may be necessary to clear the BE, BER, etc. test parameter data fields. To reset all error counters to zero, go to the BERT menu and actuate the CLR softkey. Figure 4-3 illustrates the HIGH SPEED JITTER display screen for the SWEEP mode.

8. The jitter sweep will continue from 10 HZ to 40KHZ, and will automatically reverse direction back to 10HZ, and will continue repeating the SWEEP until disabled by the operator. Each SWEEP consists of injecting jitter at the MASK amplitude for each of 106 spectral components from 10HZ to 40KHZ.

9. The BE and BER displays will indicate all detected Bit Errors and the cumulative Bit Error Rate. Framing errors, BPV's, Sync Loss Seconds, Errored Seconds, etc., may also be used in assessing jitter tolerance. The 5500 analyzer will continue to record all error parameters. The "acceptable" levels of the various error conditions are ultimately up to the customers needs and market forces. The Phoenix Model 5500 Analyzers with Model 624 T1 Interface Module and JO2 Jitter Option is required to pass this jitter tolerance SWEEP test, error free, including 24 hours burn-in at elevated temperature. Testing in other than a laboratory

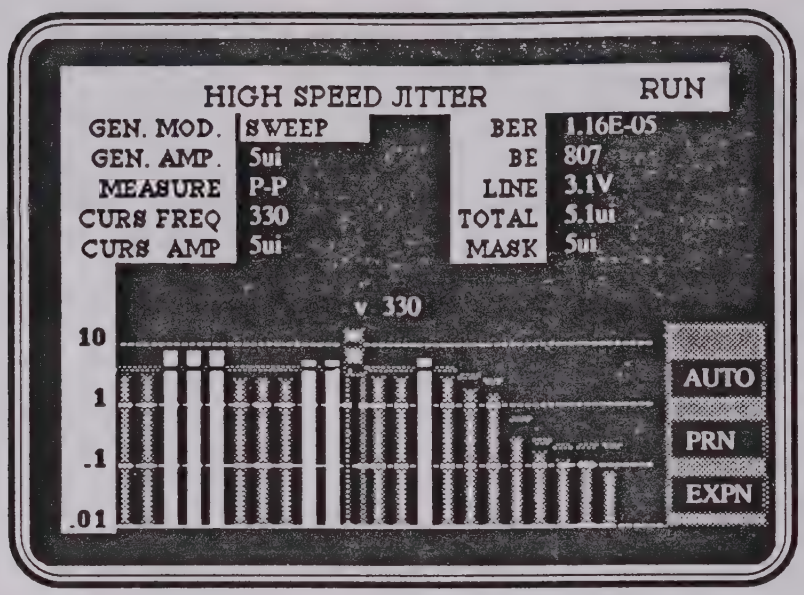


Figure 4-3. High Speed Jitter Display
Sweep Mode

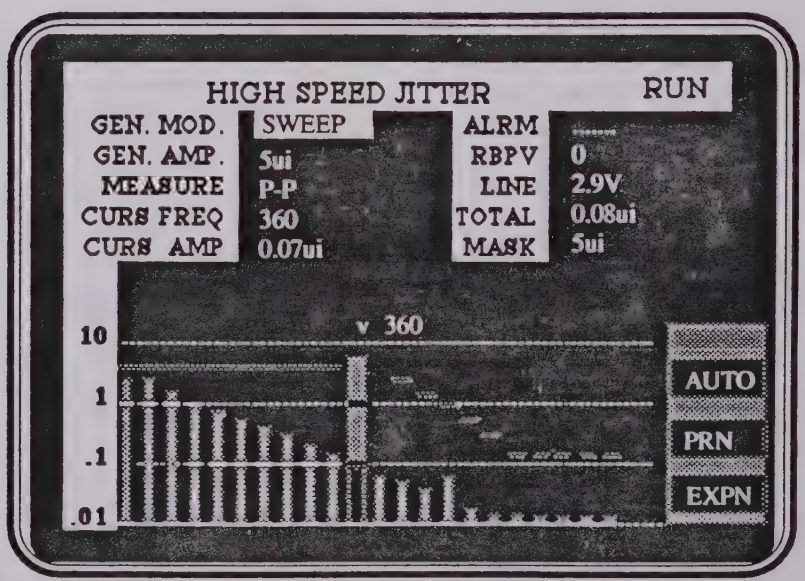


Figure 4-4. High Speed Jitter Display
Jitter Transfer Function

environment and over long haul communications facilities may necessarily require less exacting levels of performance. But in any event, the Phoenix equipment will identify degradations of performance related to phase jitter. The phase jitter graph will display the amplitude of the jitter modulation returned to the 5500 via the RX input jack. And as previously discussed, this data will be an accurate measure of the jitter transfer function, but it may not consistently correlate with jitter tolerance.

10. Select [GEN.MOD.] = SIN To allow manual control of the amplitude and frequency of the injected jitter modulation.

11. Select [CURS FREQ] = 500 500HZ is generally a good "quick look" test point to obtain a relative indication of overall jitter tolerance margins.

12. Increase [GEN AMP] from 0 ui in 0.5 ui steps, while observing the [BE] parameter block for Bit Errors. Continue adjusting the [GEN.AMP.] up (and/or down as necessary) to find the highest level of jitter modulation that can be tolerated without causing any Bit Errors (or until an acceptable Bit Error Rate is achieved, if you prefer). In some cases, the jitter tolerance of the equipment under test will exhibit hysteresis, requiring the jitter modulation to be lowered considerably before error free operation can be resumed. If the equipment will tolerate 7.5 ui of jitter at 500HZ, where the MASK limit level is 5ui, then the performance margin is 2.5ui or +50%.

13. To completely characterize the jitter tolerance margin over the entire spectrum, step the CURS FREQ and repeat the amplitude adjustment to determine the threshold of Bit Errors or acceptable Bit Error Rate at each frequency of interest.

14. By selecting the [SLOW], [EXPN] mode with the softkeys, the test frequency may be adjusted with high resolution (≅ 0.624% increments) over 1600 discrete test intervals (log spaced) across the 10HZ to 40 KHZ spectrum.

15. The ability to precisely control the frequency of modulation with 1600 step resolution may be especially important in locating the peaking frequencies in an under damped clock recovery network response to the jitter modulation.

4.3 Inject Jitter, Evaluate Jitter Transfer

Performance specifications for CSU's, multiplexers and other T1 interface devices include requirements for attenuation of phase jitter of T1 signals passed through the equipment. In troubleshooting a system or in configuring a new system to accomplish compliance with the network interface requirements, it may be necessary, and certainly advantageous, to select components whose jitter transfer attenuation characteristics compensate or compliment one another (including masking the jitter tolerance problems of downstream equipment) in the system configuration. Evaluation of the jitter transfer function of individual components, as well as the complete system, is therefore beneficial in engineering solutions to jitter compliance problems. The following set up procedure and display example illustrate the use of the Phoenix Model 5500 to measure the phase jitter transfer of T1 equipment and/or complete transmission facilities:

A) On the FRAMED T1 FORMAT menu:

1. Select LINE CODE [AMI] or [B8ZS], as required.
2. Select FRAME [ENABLE] or [DISABLE], as required
3. Select PATTERN [QRW] or other pattern, as desired
4. Select BLOCK SIZE [10^6]
5. Select BLOCKS [0] for continuous test
6. Select CLOCK SOURCE [JIT CLK]

Note: If the phase modulated JITTER CLOCK is not selected as CLOCK SOURCE, the transmitted bipolar signal will not be phase jittered.

7. Select AUTO RESYNC [ENABLE]
8. Set SOFTKEY functions to:

[BRDG] (DISABLED)

[TERM] (ENABLED)

[LOOP] (DISABLED)

B) Connect the equipment or facility under test to the TX output and RX input jacks on the rear of the model 624 interface module with JO2 option.

C) On the HIGH SPEED JITTER menu:

1. Select [GEN.MOD.] = SWEEP
2. [GEN.AMP.] level control will be automatic in this mode.
3. Select [MEASURE] = P-P
4. [CURS FREQ] contol will be automatic in this mode.
5. [CURS AMP] will display the level of phase jitter at the RX input, measured at the CURS FREQ, which is the same frequency as the modulation of the jitter clock of the transmitted data at the TX output.
6. The graph will display the amplitude bar graph of the received jitter in comparision to the MASK level of the transmitted jitter. This illustrates the jitter transfer function of the equipment under test. An example is provided in figure 4-4.
7. Numeric readouts of each spectral component may be obtained by commanding a print out of the spectrum graph and data. This data will include the reference MASK level transmitted modulation for each measurement frequency. A sample print out is presented in figure 4-5.
8. At the high end of the spectrum, in the region of 40KHZ, when measuring the level of attenuation of a 0.1 ui injected jitter modulation, the noise floor and resolution limits of the JO2 option may require the use of a higher level injected phase modulation in order to measure attenuation magnitudes as high as 20 dB. For example, if the noise floor of the jitter measurement is 0.02 ui for an injected jitter magnitude of 0.1 ui, then the maximum level of measureable attenuation is $20 \log_{10} .1/.02 = 13.98$dB. By adjusting the [GEN.AMP.] to 0.2ui in the [GEN.MOD.] SIN mode, the maximum level of measureable jitter attenuation is increased by 6dB:

$$20 \log_{10} .2/.02 = 20db$$

9. If greater dynamic range or more precise frequency resolution is required, then a spectrum analyzer can be connected to the RX MON PHASE JITTER connector on the rear of the Model 624 interface module. The output calibration scale factor of the demodulated phase jitter at this connector may be determined by measuring the demod level at a reference amplitude of 5 ui at 500HZ with the Model 5500 in LOOP mode. The amplitude of the measured phase jitter at a given modulation frequency is directly (linearly) proportional to the voltage amplitude of the demod output spectral component at that modulation frequency.

```
JITTER GENERATOR: SWEEP
TOTAL JITTER: 5.1  LINE LEVEL: 2.9V

FREQUENCY   !.01          !.1           !1            !10   AMPLITUDE   MASK
--(HZ)---   !-------------!-------------!-------------!---  --(UI)---  -(UI)-
  10      * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5.1       5
  11        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5         5
  12        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.8       5
  13        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.8       5
  14      * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5.1       5
  15      * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5.1       5
  16      * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5.3       5
  17        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.8       5
  18        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.5       5
  19        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.7       5
  20      * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5.3       5
  22      * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5.4       5
  24        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.7       5
  26        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5         5
  28        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      5         5
  30        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.7       5
  33        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.9       5
  36        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !      4.2       5
  39        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>  0    !      3.5       5
  42        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>    0    !      2.6       5
  46        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>     0    !      2.1       5
  50        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>       0    !      1.6       5
  55        +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>        0    !      1.31      5
  60        +>>>>>>>>>>>>>+>>>>>>>>>>>>>!          0    !      .91       5
  66        +>>>>>>>>>>>>>+>>>>>>>>>>>>> !         0    !      .72       5
  72        +>>>>>>>>>>>>>+>>>>>>>>>>>   !         0    !      .55       5
  79        +>>>>>>>>>>>>>+>>>>>>>>>     !         0    !      .41       5
  86        +>>>>>>>>>>>>>+>>>>>>>       !         0    !      .32       5
  94        +>>>>>>>>>>>>>+>>>>>>        !         0    !      .26       5
 100        +>>>>>>>>>>>>>+>>            !         0    !      .14       5
 110        +>>>>>>>>>>>>>+>>>           !         0    !      .16       5
 120        +>>>>>>>>>>>>>+>>            !         0    !      .14       5
 130        +>>>>>>>>>>>>>!              !         0    !      .09       5
 140        +>>>>>>>>>>>>>+              !         0    !      .1        5
 150        +>>>>>>>>>>>>>!              !         0    !      .09       5
 160        +>>>>>>>       !             !         0    !      .03       5
 170        +>>>>>>>       !             !         0    !      .03       5
 180        +>>>>>>>       !             !         0    !      .03       5
 190        +              !             !         0    !      .01       5
 200        +>>>>          !             !         0    !      .02       5
 220        +>>>>          !             !         0    !      .02       5
 240        +              !             !         0    !      .01       5
 260        +              !             !         0    !      .01       5
 280        +              !             !         0    !      .01       5
 300        +              !             !         0    !      .01       5
 330        +              !             !         0    !      .01       5
 360        +              !             !         0    !      .01       5
 390        +              !             !         0    !      .01       5
 420        +              !             !         0    1      .01       5
 460        +              !             !         0    !      .01       5
 500        +>>>>          !             !         0    !      .02       5
 550        +              !             !        0     !      .01       4.37
```

Figure 4-5. Sample Graph Printout
Sheet 1 of 2

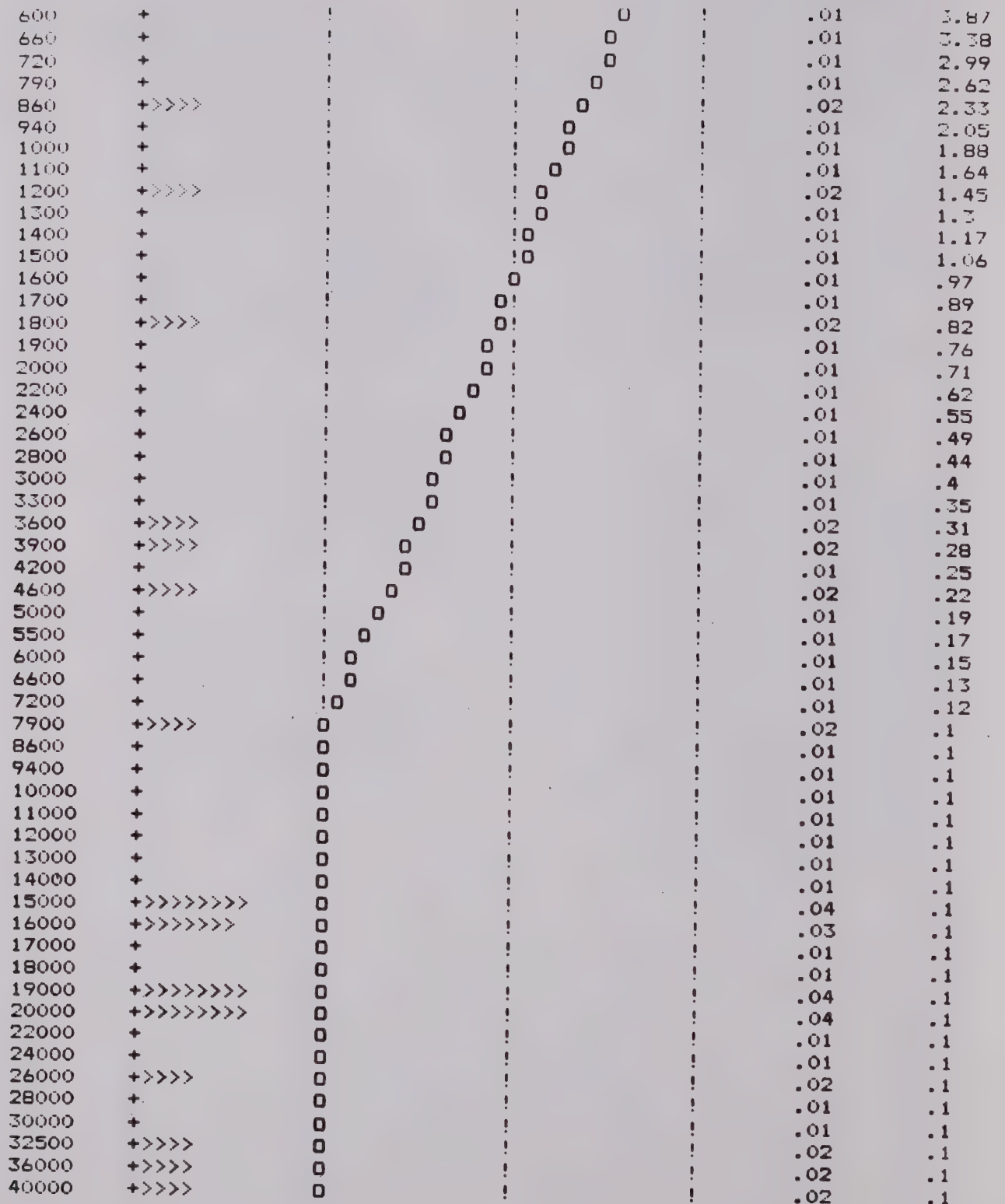


Figure 4-5. Sample Graph Printout
Sheet 2 of 2

Model 5500-900

303 Bell Interface Module

1.0 INTRODUCTION

This section details the operation of the Bell 303 Interface Module option. ASYNC, SYNC, and External modes are all self contained in the 5500. This module uses much of the same protocol as the RS-232C with minor differences. Two extra control lines were added to give the module loop and mode select capabilities. DCE or DTE emulation, and SYNC, ASYNC or external operations are controlled and switchable from the Model 5500 front panel keys, or by commands over the remote ports.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500 303 Bell Interface Module specifications.

Table 2-1. Model 5500-900 Specifications

CHARACTERISTIC	SPECIFICATION
Modes	SYNC, ASYNC, EXTERNAL
Emulation	DCE or DTE
Data Rates	75 bps to 1.544 Mbps
Character Size	5, 6, 7, 8 data bits
Parity	Odd, Even or no parity bit
Input Data Characteristics	Mark signal, binary state 2, or OFF = -3 Volts min.

2.1 FUNCTIONAL DESCRIPTION

The Bell 303 Interface Module is capable of operation in Synchronous and Asynchronous modes when configured in DTE simulation mode and Asynchronous, Synchronous and External in DCE simulation mode. The module has provisions for 2 types of connectors. A standard subminiature "D" type 15 pin connector and a 25 pin connector commonly associated with Bell System Voiceband Data Sets. The connector is equivalent to a Cinch or Cannon DB-19604-433 connector. The business machine (DTE) should be equipped with a cable not longer than 50 feet and a Cinch or Cannon DB-19604-432 plug mounted in a Cinch DB-51226-1 hood assembly. Figure 2-1 presents a simplified block diagram of the Bell 303 module. Table 2-2 presents the Bell 303 connector pin assignments.

3.0 OPERATION

3.1 DATA TERMINAL EQUIPMENT

The Model 5500 may be configured as Data Terminal Equipment (DTE) for testing Data Communications Equipment (DCE) such as modems, multiplexers, or other peripheral equipments configured in DCE. This is accomplished by toggling the front panel key labeled "DCE/DTE" until DTE appears in the upper left hand corner of the BERT CRT display (refer to section 3.2 of this instruction book for location and description of the Model 5500 controls and indicators). In the synchronous mode of operation the Model 5500 may be set to derive clock from the equipment under test or it may generate the clock internally and provide it to the equipment under test. The ALT Line is set by the DTE and sent to the DCE under test. This sets the DCE to the proper format to receive data. In this case it will expect the data to be sent in the Synchronous mode.

In the Asynchronous mode of operation data is transmitted and received without a clock; start and stop bits provide proper decoding of the data bits in each character (byte) sent, while timing is extracted from the bit transition. In Synchronous operation, with the DCE under test acting as the source of timing, the Model 5500 bit rate should be set to EXTERNAL. In this position the Model 5500 will derive clock from Pin J of the DCE I/O connector on the interface module. Transmit data and clock are available on pins E and H respectively, and receive data and clock are available on, pins K and L respectively.

If a bit rate is selected on the Model 5500 then the internal generator of the 5500 supplies the clock signal to the equipment under test. If the user desires to test a non-standard bit rate the unit can also be operated with an externally applied USER CLOCK. This clock is connected to the rear panel BNC connector with the Model 5500 Bit Rate field set to USER. The frequency of this externally applied clock is read on the CRT display by scrolling through the frequency selections to the appropriate option - either TC or BR. In either case the test set ignores the signals present on pin J of the I/O connector. Transmit data and clock are on pins E and H. Receive data and clock are on pins K and L, respectively.

When operated in an Asynchronous mode the Model 5500 bit rates are internally generated. The appropriate character size, number of stop bits, and parity must also be set using the front panel cursor and select keys. In this mode of operation no clock signals are transmitted. Transmit data appears on pins E and receive data on pin K of the I/O connectors. Any signals appearing on pins J and L are ignored. The Model 5500 recovers clock from the received data transitions to provide internal synchronization to the received patterns.

In the "Bell 303 Format" menu LOOP mode appears in the last row. This mode reflects one of two loop modes associated with this module. The "Selftest" loop mode is the normal loop mode. The "Remote" loop mode sets the loop line on the module and sends it to the DCE with instructions to loop the data back to the sender. This is a data verification technique used for analysis of random data.

3.1.1 Controls and Indicators

Model 5500 front panel controls labeled RTS/DCD and DTR/DSR enable the user to turn RTS and DTR ON and OFF when the Model 5500 is configured as DTE.

Twleve green LED's provide visual indication of the primary lead status as follows:

Transmit Data - (TD)	Data Set Ready (DSR)
Receive Data - (RD)	Data Terminal Ready (DTR)
Transmit Clock - (TC)	Data Carrier Detect - (DCD)
Receive Clock - (RC)	Ring Indicator - (RI)
Request to Send - (RTS)	Signal Quality - (SQ)
Clear to Sent - (CTS)	Transmit Clock Ext - (SCTE)

Table 2-2. Bell 303 Connector Pin Assignments

DTE Pin Number	DCE Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
						From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
X		AA	101	Protective Ground (connector body)	X						
E	4	BA	103	Transmitted Data			X				
K	1	BB	104	Received Data		X					
D	5	CA	105	Request to Send					X		
C	10	CB	106	Clear to Send				X			
F"C"	8	CC	107	Data Set Ready				X			
"O"	6	AB	102	Signal Ground (Common Return)	X						
B	14	CF	109	Received Line Signal Detector (Spare)				X			
G	15			Local Test					X		
A	13	SCB	121	Alternate					X		
I	3	DB	114	Sig. Element Timing (DCE Source)						X	
L	2	DD	115	Rec. Sig. Element Timing (DCE						X	
				Source)							
M"O"	12	CD	108.2						X		
M"C"	9	CG	110	Data Terminal Ready				X			
F"O"	11	CE	125	Signal Quality Detector				X			
				Ring Indicator							
H	7	DA	113								X

"C" = center conductor "O" = outer conductor

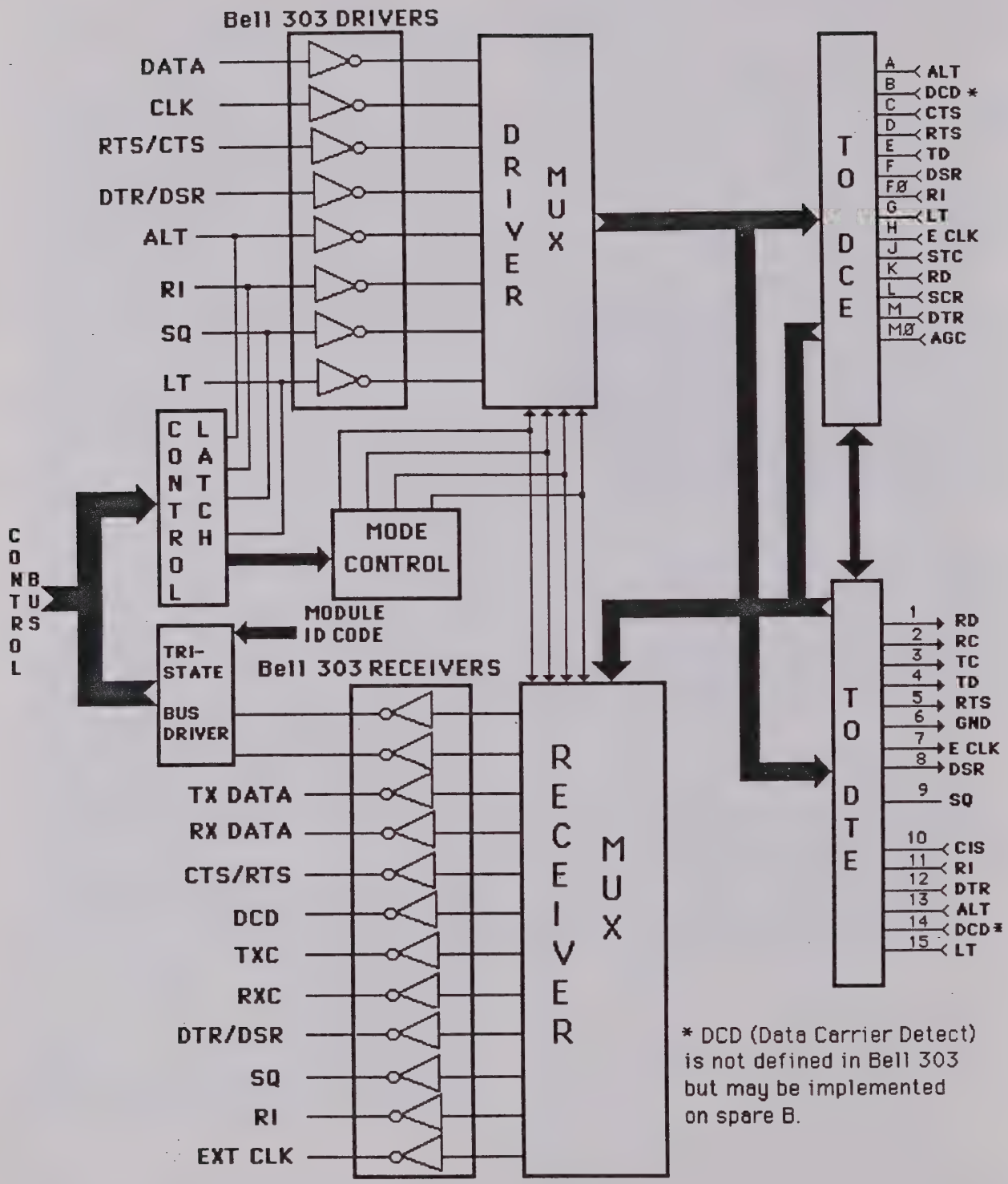


Figure 2-1. Model 5500-900 Interface Module Block Diagram

The front panel key labled DCE/DTE electronically switches the rear panel I/O connector functions from DCE to DTE and vice versa. These and any other function, and indications may accomplished and displayed at a remote terminal using the RS-232 or IEEE-488 remote control ports.

3.2 DATA COMMUNICATIONS EQUIPMENT (DCE) CONFIGURATION

The Model 5500 may also be configured to operate as a DCE by toggling the DCE/DTE front panel key until the DCE indication appears in the upper left hand corner of the CRT display. Again, either Synchronous or Asynchronous peripherals can be tested as in the DTE configuration.

In Synchronous mode, the Model 5500 may derive clock from the DTE under test or supply clock to the equipment from its own internal generator. When set to external clock, the Model 5500 receives timing from the DTE transmit signal element timing on pin 7 of the rear panel DTE I/O connector.

The frequency of the external clock is read on the CRT display by scrolling through the frequency selections to XC. Under this condition the TD on pin 4 and EXTC on pin 7 are analyzed by the Model 5500.

The Model 5500 generates RD on pin 1 and RC on pin 2 in accordance with the DTE supplied clock on pin 7.

If it is desired to have the Model 5500 supply clock for the equipment under test it is necessary to select the desired bit rate instead of EXTERNAL. In this case, the Model 5500 supplies timing to the DTE under test on pin 3 of the I/O connector. The Model 5500 analyzes the TD on pin 4 and TC on pin 3. RD on pin 1 and RC on pin 2 are generated by the Model 5500 internal clock source. A user supplied External clock signal into the User Clock BNC jack will cause the Model 5500 to generate data and clock at the externally applied clock rate when the Model 5500 is set to USER in the Bit Rate field.

Asynchronous DCE operation of the Model 5500 requires selection of the ASYNC mode, bit rate, character size, parity, and the number of stop bits. Data is generated and received in character format with no clock signals provided.

External DCE mode operation of the Model 5500 derives the signal from the ALT line on pin 13 of the DTE I/O connector. The state of this line will determine what mode the DTE is in and will set the Model 5500 (DCE) to the desired mode. User will set the desired functions correlating to this mode. Indications on this line will be on the "Bell 303 Format" menu and will be displayed "Mode [EXT - ASYNC]!
[SYNC]

3.2.1 Controls and Indicators

Front panel keys are available which enable the user to turn Data Set Ready (DSR) and Data Carrier Detect (DCD) "ON" and "OFF" in DCE mode of operation. In addition, these conditions, and any other settings can also be controlled from a remote terminal using the RS-232 or IEEE-488 rear panel remote control ports.

The twelve green LED indicators provide status of the primary interface signals leads as discussed earlier in section 3.1.1.

Remote Port Additions

CPMODE [Self Test]
[Remote]

MD [ASYNC]
[SYNC]
[EXT]

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